Analytical Model for a Tunnel Field-Effect Transistor

***Abstract*—The tunnel field-effect transistor (TFET) is a promising candidate for the succession of the MOSFET at nanometer dimensions. Due to the absence of a simple analytical model for the TFET, the working principle is generally not well understood. In this paper a new TFET structure is introduced and using Kane's model, an analytical expression for the current through the TFET is derived. Furthermore, a compact expression for the TFET current is derived and conclusions concerning TFET design are drawn. The obtained analytical expressions are compared with results from a 2D device simulator and good agreement at low gate voltages is demonstrated.**

***Index Terms*—TFET, transistor, BTBT, analytical model, Kane**

I. Introduction

As MOSFETS reach nanometer dimensions, power consumption becomes a major bottleneck for further scaling. The continued reduction of the MOSFET size is leading to an increased leakage current due to short channel effects, such as Drain Induced Barrier Lowering (DIBL), and the power supply voltage cannot be reduced any further because of the subthreshold slope being limited to 60 mV/decade at room temperature. In this view, the exploration of alternative devices which possibly outperform the MOSFET at these nanometer dimensions is required.

A promising alternative for the MOSFET, which does not suffer from these limitations, is the tunneling field-effect transistor (TFET). Throughout the rest of this paper the term TFET will not refer to any specific implementation form, but the TFET is defined as "a semiconductor device in which the gate controls the source-drain current through modulation of Band-to-Band Tunneling (BTBT)". Band-to-Band Tunneling is a process in which electrons tunnel from the valence band through the semiconductor bandgap to the conduction band or vice versa.

TFETs with a subthreshold slope lower than 60 mV/decade have already been demonstrated [1], [2] and due to their built-in tunnel barrier, Si TFETs are expected to maintain low off-currents for channel lengths down to 10 nm [3].

An advantage of TFETs compared to other alternative device concepts is that their fabrication is compatible with standard CMOS processing since they can be implemented as a reverse biased gated p-i-n diode. Moreover, compared to for example the I-MOS [4], TFETs do not rely on high energetic processes like impact ionization, which are known to be detrimental to reliability.

Contrary to the MOSFET and the bipolar transistor, the TFET does not have a simple analytical model. This hampers a clear understanding of the TFET working principle.

In this paper, an analytical model for a TFET is developed. First a new TFET device structure is presented for which the potential profile can be determined straightforwardly. As a result, the total current through the device can be calculated analytically, as shown in Section II. In order to obtain a closed expression for the current, an approximation regarding the behavior of the current around the BTBT onset voltage needs to be made, as discussed in Section III. The calculations originating from the analytical expression are validated in Section IV by comparing them with device simulator results.

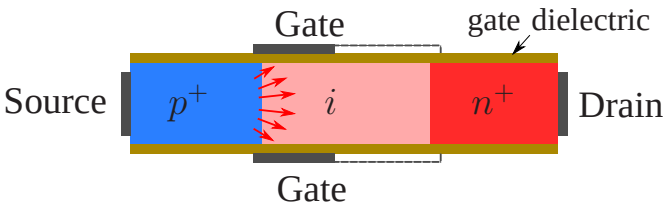

Fig. 1. Double gate TFET with full (solid) and short (dashed) gate respectively as shown in [5], the direction of BTBT in the semiconductor is indicated by arrows

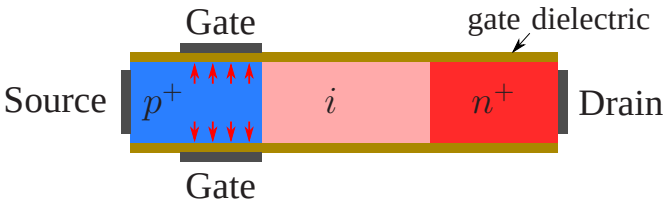

Fig. 2. New device concept which enables derivation of an analytical model, the direction of BTBT in the semiconductor is indicated by arrows

II. Analytical Model

A. Device structure

The TFET is generally described as a gated p-i-n diode. Investigations [5] have shown that the gate does not need to cover the entire intrinsic region but can be restricted to the area close to the source. A double gate TFET is shown in Fig. 1 illustrating the full and the short gate concept. Neither of these structures allow for a simple analytical expression for the electric field and the electrostatic potential throughout the device. This hampers an analytical treatment that would give insight into the working principle of the device.

In this paper a new TFET configuration is presented such that the gate is located fully on top of the source as illustrated in Fig. 2. The device can be regarded as an extreme case of the short gate TFET as the gate does not even cover a part of the channel. It is important to note that in this device, the BTBT occurs in the direction orthogonal to the gate. The one-dimensional nature of the BTBT enables an approximate determination of the potential profile in the tunneling region.

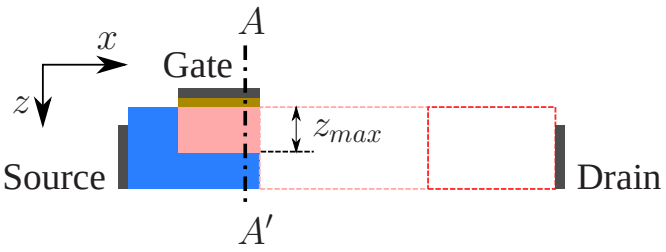

Fig. 3. TFET from Fig. 2 with positive gate bias applied such that a depletion region with thickness $z_{\max}$ exists (only upper half shown)

The derivation of the current formula in this paper is restricted to the case of an nTFET, i.e. the gate is located on top of the p-type source. An analogous calculation can be made for a pTFET with an n-type source.

B. Potential profile

Whereas the gate strictly controls the electrostatic potential in the underlying semiconductor, the influence of the drain voltage is found to be weak and can be neglected in the region directly under the gate.

Under the assumption that there is no substantial potential variation in the direction parallel to the gate, the potential profile can be considered one-dimensional. Adopting the depletion layer approximation, the electric field and the electrostatic potential in the semiconductor are written in terms of the acceptor doping concentration of the source (N_{a}) [6]:

$$\psi(z) = \frac{qN_{\mathrm{a}}}{2\epsilon_{\mathrm{s}}}\left(z - z_{\max}\right)^2 \tag{1}$$

$$E_z(z) = -\frac{qN_{\mathrm{a}}}{\epsilon_{\mathrm{s}}}\left(z - z_{\max}\right) \tag{2}$$

where $z_{\max}$ is the length of the depletion region, which is a function of the applied gate voltage. q is the elementary electric charge and ϵ_{s} is the permittivity of the semiconductor.

C. Current

Since a p-i-n diode in reverse bias is considered, the current is small if no BTBT is present, in which case the current is referred to as the off-current. As soon as BTBT occurs however, the resulting on-current will dominantly exceed the off-current.

In semi-classical simulators, BTBT is modelled by the introduction of an extra generation term (G) in the drift-diffusion equation. When the BTBT current contribution is dominating, the TFET current can be computed as the sum over all charge generated in the device:

$$|I| = q\int G\mathrm{d}V = qWL\int G\mathrm{d}z \tag{3}$$

with $\mathrm{d}V$ an elementary volume in the device, L and W the gate length and width respectively and G the generation rate expressed in number of carriers per unit volume per unit time. In Eq. 3 translational invariance in the y-direction is assumed and the variation of the generation rate in the x-direction is neglected.

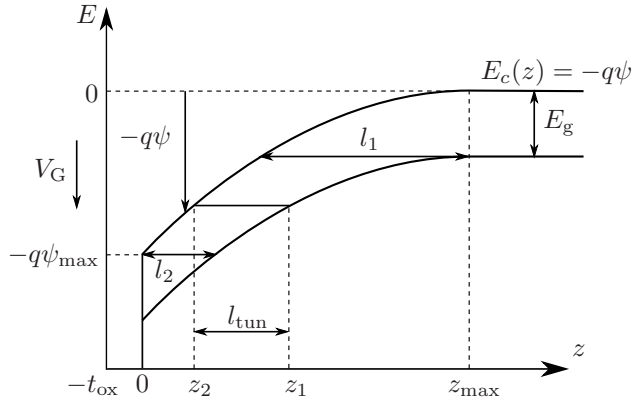

Fig. 4. Band diagram of the cross-section A-A' from Fig. 3 indicating l_{tun}

The most popular model to calculate the generation is Kane's Model [7]. Kane's model is derived for a direct semiconductor in a uniform electric field and is given by:

$$G(E) = A\frac{E^D}{\sqrt{E_{\mathrm{g}}}}\exp\left(-B{E_{\mathrm{g}}}^{3/2}/E\right) \tag{4}$$

where E is the electric field and E_{g} the bandgap, while A and B are parameters depending on the effective mass of valence and conduction bands and D takes a default value of 2, but for the sake of generality it is left unspecified as an adjustable parameter.

The effect of the different regions arising when a positive gate voltage is applied, is discussed in the following subsections.

1) Neutral region: The neutral region is characterized by the absence of an electric field and does not contribute to the BTBT current.

2) Depletion region: In this section, the current is calculated assuming that there is only a depletion region. Instead of relying on the local electric field as in Refs. [8], [9], we insert the average electric field over the tunnel path into the Kane generation rate. A similar strategy is followed by some commercial device simulators [10]. Accordingly, a more accurate estimate of the current can be made, and the tunnel current disappears in a natural way when no tunnel path is available due to the average electric field being zero.

The tunnel path is defined as the physical path between two points corresponding to equal energy for the conduction and valence band respectively. The average field in the z-direction ($\bar{E}_z$) is then given by:

$$\bar{E}_z = \frac{E_{\mathrm{g}}}{ql_{\mathrm{tun}}} \tag{5}$$

with E_{g} the bandgap energy and l_{tun} the length of the tunnel path.

To calculate l_{tun}, the z-coordinate of points of equal potential in valence and conduction band are considered. Writing,

$$\psi_v(z_1) = \frac{qN_{\mathrm{a}}}{2\epsilon_{\mathrm{s}}}(z_1 - z_{\max})^2 + \frac{E_{\mathrm{g}}}{q} \tag{6}$$

$$\psi_c(z_2) = \frac{qN_{\mathrm{a}}}{2\epsilon_{\mathrm{s}}}(z_2 - z_{\max})^2 \tag{7}$$

from which the tunnel path length can be determined:

$$l_{\mathrm{tun}} = z_1 - z_2 \tag{8}$$

$$\psi_v(z_1) = \psi_c(z_2) \tag{9}$$

Writing z_2 as a function of l_{tun},

$$z_2 = z_{\max} - \frac{1}{2}\frac{l_{\mathrm{tun}}^2 + 2E_{\mathrm{g}}\epsilon_{\mathrm{s}}/(q^2 N_{\mathrm{a}})}{l_{\mathrm{tun}}} \tag{10}$$

this yields following expression for $\mathrm{d}z$:

$$\mathrm{d}z = -\frac{1}{2}\left(1 - \frac{2E_{\mathrm{g}}\epsilon_{\mathrm{s}}}{q^2 N_{\mathrm{a}}}\frac{1}{l_{\mathrm{tun}}^2}\right)\mathrm{d}l_{\mathrm{tun}} \tag{11}$$

Substituting Eqs. (4), (5) and (11) into Eq. (3):

$$I = \frac{qWLA}{2}\int_{l_1}^{l_2}\frac{E_{\mathrm{g}}^{D-\frac{1}{2}}}{q^D l_{\mathrm{tun}}^D}e^{-Bq\sqrt{E_{\mathrm{g}}}l_{\mathrm{tun}}}\left(1 - \frac{2E_{\mathrm{g}}\epsilon_{\mathrm{s}}}{q^2 N_{\mathrm{a}}}\frac{1}{l_{\mathrm{tun}}^2}\right)\mathrm{d}l_{\mathrm{tun}} \tag{12}$$

l_1 and l_2 respectively denote the maximal and minimal length of the tunnel path in the depletion region:

$$l_1 = \sqrt{\frac{2E_{\mathrm{g}}\epsilon_{\mathrm{s}}}{q^2 N_{\mathrm{a}}}} \tag{13}$$

$$l_2 = \sqrt{\frac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{a}}}}\left(-\sqrt{\psi_{\max} - \frac{E_{\mathrm{g}}}{q}} + \sqrt{\psi_{\max}}\right) \tag{14}$$

$\psi_{\max}$ is the potential at the end of the depletion region as indicated in Fig. 4.

Integration by parts reduces the integral in (12) to a logarithmic integral, that cannot be evaluated analytically.

3) Inversion layer: The gate voltage specifying the onset of inversion is given by the well-known expression:

$$V_{\mathrm{GS}} = V_{\mathrm{FB}} + 2\phi_f + \Phi_n + \frac{t_{\mathrm{ox}}}{\epsilon_{\mathrm{ox}}}\sqrt{2qN_{\mathrm{a}}\epsilon_{\mathrm{s}}}\sqrt{\Phi_n + 2\phi_f} \tag{15}$$

where Φ_n is the electron quasi-Fermi level relative to the source voltage, V_{FB} is the flatband voltage, $\phi_f = \ln(N_{\mathrm{a}}/n_i)\,kT/q$ is the surface potential, t_{ox} is the oxide thickness and ϵ_{ox} is the dielectric constant of the oxide.

The respective positions of the quasi-Fermi levels also determine the ratio between BTBT generation and BTBT recombination. In the previous treatment for the depletion region the respective positions of the quasi-Fermi levels were ignored and BTBT was entirely attributed to generation. This is an acceptable approximation as long as the valence band is filled and the conduction band is empty.

In the case of a non-degenerate semiconductor, the inversion regime sets in before the electron quasi-Fermi level and the conduction band meet. In the depletion region, only the tail of the Fermi-Dirac distribution occupies the conduction band which is negligible compared to the almost fully occupied valence band. In the inversion layer however, the conduction band is filled and BTBT recombination can no longer be neglected.

However, the inversion layer, being small in size and having only a small generation rate, only gives rise to a small contribution to the total current and therefore its contribution is neglected in this paper.

4) Total current: Using the previous approach, the total current in the device equals the current generated in the depletion region. The influence of the gate voltage is straightforward, namely increasing the depletion region size and increasing the current accordingly. The drain voltage determines the onset of inversion and therefore imposes an upper limit to the depletion region size through Eq. (15).

In a degenerate semiconductor, the limits l_1, l_2 of the integration (12) need to be altered such that the integration only extends over the region of tunneling where the conduction band is (approximately) empty and the valence band is (approximately) full.

III. Approximating formula

A. Derivation

In order to further elaborate on Eq. (12) it is assumed that the exponential terms change much more rapidly than the polynomial terms under a variation of l_{tun}. Approximating the integral and inserting Eq. (13), an expression for the current as a function of l_2 is derived:

$$I \approx -\frac{WLAE_{\mathrm{g}}^{D-1}}{2Bq^D}\left(\frac{1}{l_2^D} - \frac{2E_{\mathrm{g}}\epsilon_{\mathrm{s}}}{q^2 N_{\mathrm{a}}}\frac{1}{l_2^{D+2}}\right)e^{-Bq\sqrt{E_{\mathrm{g}}}l_2} \tag{16}$$

Next, $\psi_{\max}$ is calculated as a function of the applied gate voltage V_{G}. V_{G} can be written as the sum of the electrostatic potential at the interface ($\psi_{\max}$) and the potential difference over the oxide,

$$V_{\mathrm{GS}} - V_{\mathrm{FB}} = \psi_{\max} + t_{\mathrm{ox}}E_{\mathrm{ox}} \tag{17}$$

Since no potential change along the x-direction is considered, the electric field has only a component in the z-direction. The oxide electric field (E_{ox}) can be calculated from the semiconductor electric field (E_{s}) by making use of the boundary condition at the interface: $\epsilon_{\mathrm{ox}}E_{\mathrm{ox}} = \epsilon_{\mathrm{s}}E_{\mathrm{s}}$.

The electric field changes linearly in the depletion region while the electrostatic potential changes quadratically according to Eqs. (1) and (2). Writing the gate voltage as a function of $\psi_{\max}$:

$$V_{\mathrm{GS}} - V_{\mathrm{FB}} = \psi_{\max} + 2t_{\mathrm{ox}}\frac{\epsilon_{\mathrm{s}}}{\epsilon_{\mathrm{ox}}}\sqrt{\frac{qN_{\mathrm{a}}}{2\epsilon_{\mathrm{s}}}\psi_{\max}} \tag{18}$$

Combining Eqs. (18), (16) and (14) is useful for comparison of the analytical model with simulation results. The resulting formula however, is rather involved and still hampers a straightforward conclusion. We may however gain more insight by calculating the current in the neighborhood of the TFET onset voltage V_{onset} which marks the onset of BTBT in the depletion region, or equivalently, the band bending being equal to the bandgap, $\psi_{\max} = E_{\mathrm{g}}/q$. Hence,

$$V_{\mathrm{onset}} = V_{\mathrm{FB}} + \frac{E_{\mathrm{g}}}{q}\left(1 + 2t_{\mathrm{ox}}\frac{\epsilon_{\mathrm{s}}}{\epsilon_{\mathrm{ox}}}\sqrt{\frac{q^2 N_{\mathrm{a}}}{2E_{\mathrm{g}}\epsilon_{\mathrm{s}}}}\right) \tag{19}$$

Calculating the current given by Eq. (16) for $\psi_{\max} = E_{\rm g}/q + \delta\psi$ where $\delta\psi$ is a perturbation of the electrostatic potential, we arrive at:

$$I \approx \frac{WLA\sqrt{q}}{BE_{\rm g}^{3/2}} \left(\frac{E_{\rm g}N_{\rm a}}{2\epsilon_{\rm s}}\right)^{D/2} e^{Bq\sqrt{2\epsilon_{\rm s}E_{\rm g}}/\sqrt{qN_{\rm a}}(\sqrt{\delta\psi}-\sqrt{E_{\rm g}/q})}\sqrt{\delta\psi} \tag{20}$$

Writing $\delta\psi$ as a function of the gate voltage:

$$\delta\psi = (V_{\rm GS} - V_{\rm onset})/\gamma \tag{21}$$

$$\gamma = 1 + t_{\rm ox}\frac{\epsilon_{\rm s}}{\epsilon_{\rm ox}}\sqrt{\frac{q^2N_{\rm a}}{2E_{\rm g}\epsilon_{\rm s}}} \tag{22}$$

we obtain a closed formula for $D = 2$,

$$I \approx WLTe^{S\sqrt{V_{\rm GS}-V_{\rm onset}}}\sqrt{V_{\rm GS}-V_{\rm onset}} \tag{23}$$

with

$$T = q\frac{A}{Bq^{3/2}}\frac{qN_{\rm a}}{2\epsilon_{\rm s}}\sqrt{\frac{1}{E_{\rm g}\gamma}}e^{-BqE_{\rm g}\sqrt{2\epsilon_{\rm s}}/\sqrt{q^2N_{\rm a}}} \tag{24}$$

$$S = Bq\sqrt{\frac{2E_{\rm g}\epsilon_{\rm s}}{qN_{\rm a}}\frac{1}{\gamma}} \tag{25}$$

B. Interpretation

Eq. (23) provides the on-current in the TFET as a function of gate voltage when the device parameters are known. Clearly, the square root dependence indicates the absence of a 60 mV/decade subthreshold slope.

The influence of the different parameters on the prefactor T (Eq. (24)) and the onset voltage $V_{\rm onset}$ (Eq. (19)) is illustrated in table I and will be discussed next. The prefactor T in front of the exponential rather than the exponential itself is considered, as it determines the current in the nearest neighborhood of the onset voltage.

The bandgap is one of the most important parameters when considering a TFET, since it determines the "barrier" between valence and conduction band. The on-current increases with decreasing bandgap as indicated by Eq. (24), while also $V_{\rm onset}$ is reduced since the voltage required to create a path from valence to conduction band is directly proportional to the bandgap. A small bandgap is therefore beneficial for a large TFET on-current and is desirable as far as it does not jeopardize the TFET off-current.

It is however important to keep in mind that Eq. (23) is derived using Kane's model which applies to a direct semiconductor in a uniform field. For an indirect semiconductor a more precise treatment is required. In addition, quantization effects due to the small size of the depletion region that were not considered in this work, should also be taken into account.

A higher doping level of the source increases the on-current. This can be understood by realizing that the doping level determines the curvature of the potential in the depletion region. A larger doping level will thus decrease the tunnel distance and increase the current. An upper limit on the onset voltage or on the voltage drop over the oxide will limit the doping level.

TABLE I
EXAMPLE VALUES FOR T AND $V_{\rm onset}$

Doping level ($\rm cm^{-3}$)	Bandgap (eV)	T ($\rm Acm^{-2}V^{-1/2}$)	$V_{\rm onset}$ (V)
10^{19}	1	$1.3 \cdot 10^{-4}$	1.2
10^{19}	0.5	66	0.64
$2 \cdot 10^{19}$	1	0.5	1.3
$2 \cdot 10^{19}$	0.5	$5.6 \cdot 10^{3}$	0.7
10^{20}	1	$4.9 \cdot 10^{4}$	1.6
10^{20}	0.5	$3.9 \cdot 10^{6}$	0.95

The oxide thickness has little impact on the on-current while its influence on the onset voltage is straightforward. I.e. a smaller oxide thickness reduces the voltage drop over the oxide and reduces the onset voltage. A small oxide thickness is required to enable the gate to adequately control the source region and it will therefore improve the validity of the approximations.

Finally it is important to notice that Eq. (23) has been derived for the structure shown in Fig. 2. The conclusions drawn in this section cannot be directly applied to a general TFET structure, although the working principle remains the same.

IV. COMPARISON WITH SIMULATION RESULTS

To obtain Eq. (12) and the formulas thereafter a number of assumptions had to be made: the TFET current was restricted to the dominating BTBT contribution in the depletion region under the source. It is however not proven that the BTBT contribution in the channel or the inversion layer contribution are negligible.

In order to verify the above approximations, the derived formulas (12) and (23) are calculated numerically and compared with simulation results.

In Fig. 5 and Fig. 6 the current calculated by the analytical model and the current calculated by Medici [10], both in a self-consistent and a non-selfconsistent way, are shown. The non-selfconsistent current calculation implies a self-consistent solution of the drift-diffusion equations without taking BTBT into account. Based on the potential profile calculated in this way, the total amount of BTBT is calculated which is then identified with the total current.

The analytical results agree very well with the non-selfconsistent calculations by Medici. For large gate voltages, the (more accurate) self-consistent calculation of the current shows a difference, because the electron quasi-Fermi level under the gate has been assumed constant and equal to the drain voltage.

The electrons generated due to BTBT are bound to flow towards the drain, which may cause a significant drop of the electron quasi-Fermi level between the position where the generation takes place and the drain, and can be thought of as a series resistance. The latter depends on the mobility, thickness and length of the channel. The series resistance interpretation can be verified in Fig. 6 where simulations for different oxide thicknesses are compared.

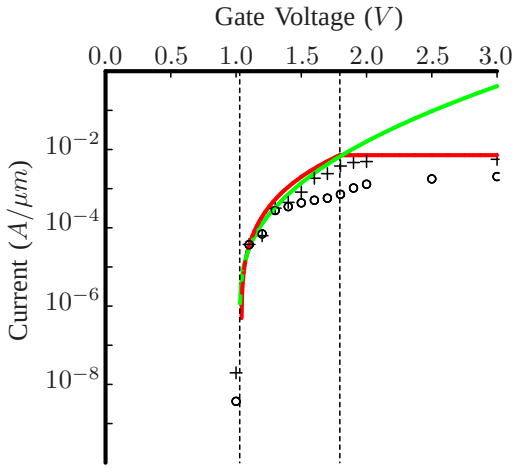

Fig. 5. Self-consistent simulations (○) and non-selfconsistent simulations (+) compared with analytical formulas (12) (▬) and (23) (▬) with the gate voltage of the former limited according to Eq. (15).

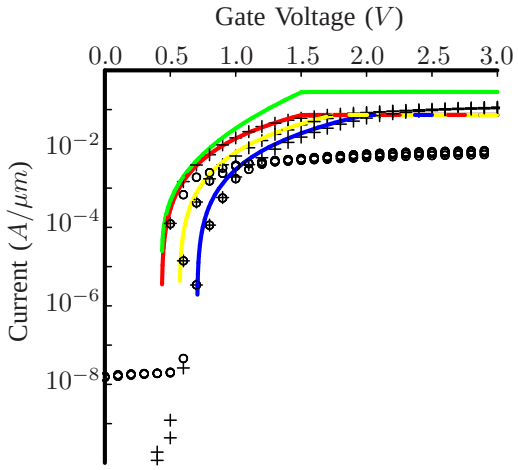

Fig. 6. Self-consistent simulations (○) and non-selfconsistent simulations (+) compared with analytical formula (12) for an oxide thickness of 2 nm (▬), 3 nm (▬) and 4 nm (▬) and formula (23) for 2 nm (▬) with the gate voltage limited according to Eq. (15).

V. Conclusion

By considering a TFET structure with a gate on top of the source, it is possible to obtain an analytical description of the potential profile in the TFET. Using this potential profile and adopting Kane's Model, we derived an analytical expression for the on-current. The approximations accompanying this derivation are justified by comparison with numerical simulation results.

The compact expression for the current shows the impact of the doping level, bandgap and oxide thickness on the TFET on-current.

For the design of a TFET as introduced in this paper, a small bandgap and a high doping level of the source are beneficial to achieving a high on-current. But the bandgap cannot be reduced indefinitely because of the off-current whereas the doping level is also limited by the TFET onset voltage. A small oxide thickness improves the validity of the approximations which were made.

Appendix A
Parameters used

A. Medici parameters used for Fig. 5

Semiconductor material: Silicon
Gate dielectric: HfO2 $t_{ox} = 2\,\mathrm{nm}$
Source doping: uniform p-type $10^{20}\,\mathrm{cm}^{-3}$
Channel doping: uniform n-type $10^{13}\,\mathrm{cm}^{-3}$
Drain doping: uniform n-type $10^{19}\,\mathrm{cm}^{-3}$
Gate workfunction: (Si) Neutral
Models: BTBT BT.MODEL=3 BGN (self-consistent)
Models: ˆBTBT (non-selfconsistent)
Gate length (L): $24\,\mathrm{nm}$
Drain voltage (V_{DS}): $0.5\,\mathrm{V}$
Channel length: $8\,\mathrm{nm}$

B. Medici parameters used for Fig. 6

Semiconductor material: Semicond $0.5\,\mathrm{V}$ ($0.38\,\mathrm{V}$ after BGN), mobility $10^4\,\mathrm{cm}^2/(\mathrm{Vs})$
Gate dielectric: HfO2 $t_{ox} = 2/3/4\,\mathrm{nm}$
Source doping: uniform p-type $5 \cdot 10^{19}\,\mathrm{cm}^{-3}$
Channel doping: uniform n-type $10^{13}\,\mathrm{cm}^{-3}$
Drain doping: uniform n-type $10^{19}\,\mathrm{cm}^{-3}$
Gate workfunction: (Si) Neutral
Models: BTBT BT.MODEL=3 BGN (self-consistent)
Models: ˆBTBT (non-selfconsistent)
Gate length (L): $24\,\mathrm{nm}$
Drain voltage (V_{DS}): $0.5\,V$
Channel length: $45\,\mathrm{nm}$

C. Device parameters used for Table I

Gate dielectric: $t_{ox} = 2\,\mathrm{nm}$
Flatband Voltage: $V_{\mathrm{FB}} = 0\mathrm{V}$
BTBT parameters: $A = 3.5 \cdot 10^{21}\,(\mathrm{eV})^{1/2}/(\mathrm{cm} \cdot \mathrm{s} \cdot \mathrm{V}^2)$, $B = 22.5 \cdot 10^6\,\mathrm{V}/(\mathrm{cm} \cdot (\mathrm{eV})^{3/2})$
Dielectric constants: $\epsilon_{\mathrm{s}} = 11.8\epsilon_0$, $\epsilon_{\mathrm{s}} = 21\epsilon_0$

References

[1] J. Appenzeller, Y.-M. Lin, J. Knoch, Z. Chen, and P. Avouris, "Comparing carbon nanotube transistors - the ideal choice: a novel tunneling device design," *Electron Devices, IEEE Transactions on*, vol. 52, no. 12, pp. 2568–2576, December 2005.

[2] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mv/dec," *Electron Device Letters, IEEE*, vol. 28, pp. 743–745, Aug. 2007.

[3] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel fet with tunnel bandgap modulation and gate workfunction engineering," *IEEE Transactions on Electron Devices*, vol. 52, no. 5, May 2005.

[4] K. Gopalakrishnan, P. Griffin, and J. Plummer, "Impact ionization MOS (I-MOS)-Part I: device and circuit simulations," *Electron Devices, IEEE Transactions on*, vol. 52, no. 1, pp. 69–76, January 2005.

[5] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "A tunnel field-effect transistor without gate-drain overlap," *Applied Physics Letters*, vol. 91, no. 053102, July 2007.

[6] S. Sze, *Physics of Semiconductor Devices*, 2nd ed. John Wiley & Sons, 1981.

[7] E. O. Kane, "Zener tunneling in semiconductors," *Journal of Physics and Chemistry of Solids*, vol. 12, pp. 181–188, 1959.

[8] T. Chan, J. Chen, P. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," *Electron Devices Meeting, 1987 International*, vol. 33, pp. 718–721, 1987.

[9] A. Qin Zhang; Wei Zhao; Seabaugh, "Low-subthreshold-swing tunnel transistors," *Device Letters, IEEE*, vol. 27, no. 4, pp. 297–300, April 2006.
[10] *Medici User Guide*, Synopsis, March 2007.