Design of an integrated CMOS PLL frequency synthesizer

***Abstract*—Due to higher costs, bulkiness and larger power consumption, it is no longer desirable to implement wireless transceivers with discrete elements. This paper describes the design of an essential component in wireless transceivers, the frequency synthesizer. The synthesizer is implemented using the dual phase locked loop (PLL) architecture. The synthesizer generates signals in the 2.4-2.5 GHz range with a 1 MHz resolution. Using the 0.35 µm CMOS process, post-layout simulations showed a phase noise of –82 dBc/Hz at an offset of 10 kHz and reference sidebands at -60 dBc, both these parameters with respect to a 2.45 GHz carrier.**

***Index Terms*—frequency synthesizer, phase locked loop (PLL), voltage controlled oscillator (VCO), single sideband (SSB) mixer, ring oscillator, skewed delay, LC oscillator, on-chip inductor, pn-junction varactor.**

I. Introduction

WIRELESS communication has undergone an incredible development over the past decades. In order to meet a growing demand for mobile wireless communication, it is desirable to implement some transceivers monolithically with the help of improving large-scale low-cost integration technology. CMOS technology is preferred because of the possibility to offer the lowest cost solution; furthermore it has the potential to realize the addition of digital function with the front-end circuit. However, due to the high-frequency parasitic effects and high noise of standard digital CMOS process, all-CMOS transceivers were only recently implemented. One of the main challenges in an all-CMOS transceiver is the design of an on-chip low-noise frequency synthesizer. Due to the close separation between the channels in wireless communication systems, RF synthesizers employed in wireless transceivers have very stringent frequency specifications and have restrictive phase noise requirements to reduce the effect of other large blocking signals as discussed in [1].

This paper is formatted to discuss the complete design of the synthesizer using the approach presented in [2], viz. from the design specifications (section II) ⇒ concept designs (section III) ⇒ subsystems (section IV) ⇒ simulation results (section V) and eventually conclusion (section VI).

II. Design Specifications

In RF transceivers, a frequency synthesizer generates the periodic signals required for both upconversion and down-conversion. Some of the main design specifications and considerations [3] are as follows.

A. Output frequency range and resolution

The frequency synthesizer must generate signals with frequencies in the 2.4-2.5 GHz range. This frequency range is commonly used for various Industry, Scientific and Medicine (ISM) applications. Considering the close separation between the channels in developing wireless communication systems as well as closely tied PLL architectural trade-offs, a frequency resolution of at least 1 MHz was chosen.

B. Phase noise

For an ideal oscillating source, a sharp impulse is expected in the frequency spectrum. However, due to random fluctuations in the oscillating source, expressed in terms of phase noise, the spectrum exhibits "skirts" around the carrier. As discussed in [1], [3], the finite phase noise corrupts both the upconverted and downconverted signals. Furthermore, as shown in fig. 1, there may also be large interferers in adjacent channels, which may be quite close to the desired signal. When the desired signal and the interferer are mixed with non-ideal LO output signal, the tail of the interferer spectra corrupts the down-converted signal band of interest and thus reduces the signal-to-noise ratio (SNR). This effect is called "reciprocal mixing". In the transmitter, large-power transmitted signals with substantial phase noise can corrupt weak nearby signals.

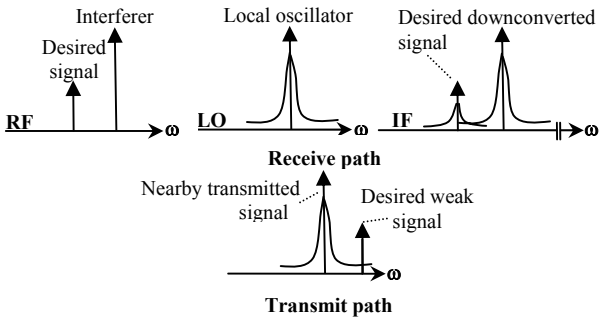

Fig. 1. Effect of phase noise on receive and transmit paths.

As shown in [4], the rather smaller Q obtained from on-chip inductors is one of the main factor that deteriorates the phase noise. The numerical specification of phase noise is often application dependent, for this design a typical value of -80 dBc/Hz was chosen.

C. Spurious frequencies

Furthermore, sidebands or spurious frequencies, which are deterministic non-ideal components in the output spectrum, are also generated. Sidebands have a particularly troublesome effect [3] in the receive path, this is as the downconverted interferer may possibly fall in the desired channel. Typical systems require that all sidebands be approximately 60 to 70 dB below the carrier, introducing a trade-off between sideband suppression and switching speed in phase locked loop topologies.

D. Switching time

The output frequency may be controlled via a channel table set by a pseudorandom number generator as in an application using frequency hopping spread spectrum (FHSS). A finite time is required to establish the output frequency; this should be such that the other transceiver subsystems need not have to "wait" for the synthesized frequency. The switching time varies from architecture to architecture, the dual PLL topology selected (section III), shows a remarked improvement in switching time as compared to traditional single loop integer-*N* PLL topology. An initial design switching time of less than 1 ms was aimed.

III. CONCEPT DESIGNS

Traditionally, synthesizers have been implemented using direct techniques such as the direct digital synthesizer (DDS) or the direct analog synthesizer (DAS). However, these designs often end up involving numerous components and hence are not suitable for monolithic RF transceivers. This is one of the main reasons why the PLL (indirect synthesizer) became the dominant architecture for frequency synthesis. Within this architecture several topologies have been developed.

A. Simplest topology: Single loop Integer-N PLL

This topology entails of a simple PLL with an integer-*N* programmable divider in the feedback path as shown in fig. 2.

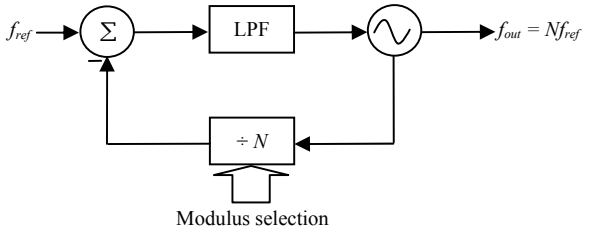

Fig. 2. Block diagram of a single loop integer-*N* topology.

Due to simplicity, this topology is commonly used - however, it suffers from a number of drawbacks. As discussed in [3], the output frequency changes by only integer multiples of the reference frequency, hence the close spacing in wireless communication systems limits the reference frequency and the loop bandwidth. The periodic disturbance of the VCO control due to the sampling action of the reference frequency in the phase detector creates further unwanted sidebands in the VCO output and, it places further limitation on the loop bandwidth. Many techniques have been proposed to overcome the trade-off among frequency division ratios, loop bandwidth and reference frequency.

B. An improved topology: the fractional-N topology

In fractional-*N* synthesizers, as shown in fig.3, the divider architecture is modified in order to obtain frequency change by a fraction of the reference frequency. Therefore, the tradeoff in the PLL synthesizer with an integer divider does not apply to fractional-*N* synthesis. The modification allows a larger loop bandwidth compared to that in the case of an integer-*N* topology under the same channel separation [1]. Thus, it increases the locking speed of the synthesizer and provides more suppression of the VCO output phase noise close to the carrier. The drawback is the existence of large fractional sidebands at the output and location of the spurs vary with the divide value. Techniques such as noise shaping by S-Δ modulation for spur reduction have been proposed [1], however these further complicate the design of this topology.

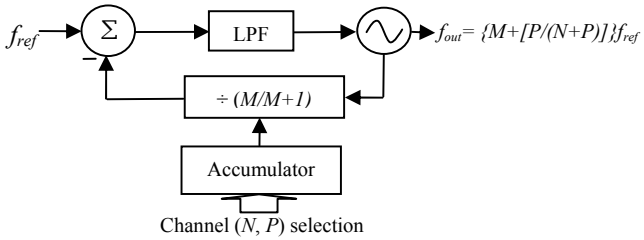

Fig. 3. Block diagram of a fractional-*N* topology.

C. Further improved/optional topology: Dual-loop topology

Employing two or more loops can alter the relationship between the channel spacing and the reference frequency of integer-*N* synthesizers as discussed in [4]. Two loops, just like any two circuit elements, may be combined in either series or parallel. The loops are combined by means of a SSB mixer. SSB mixers are usually highly nonlinear and exhibit large spurs on its output. Hence, a clever choice of placing the mixer may improve the eventual output from the synthesizer. As proposed in [1, if the SSB mixer is placed within one of the loops (fig. 4) rather than on the output of the two loops (fig. 5), the desired synthesized signal quality can be remarkably improved. The synthesizer focused in this paper uses the earlier (dual loops connected in series) proposal, despite that the loop requires a longer time to settle, the sidebands from the mixer are greatly attenuated is a bigger advantage.

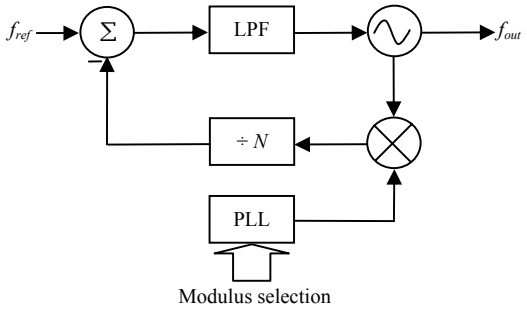

Fig. 4. Block diagram of a dual (series connected) loop topology with the SSB mixer placed within the upper-loop.

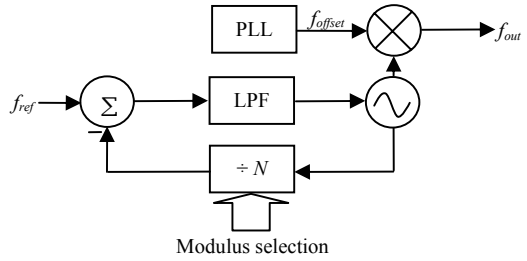

Fig. 5. Block diagram of a dual (parallel connected) loop topology with the SSB mixer placed on the output of the two synthesizers.

It is further shown in [1] that placing a prescaler (÷ X) as in fig. 6, helps to attenuate the sidebands resulting from the reference source of the lower loop. Each divide-by-2 counter can provide 6 dB reduction of phase noise of its output carrier comparing to its input, and thus the chosen value of X = 4, provides approximately 12 dB reduction of phase noise of the lower loop output signal. Fig. 6 also shows a complete frequency planning of the system with certain important subsystem (detailed in section III) specifications indicated.

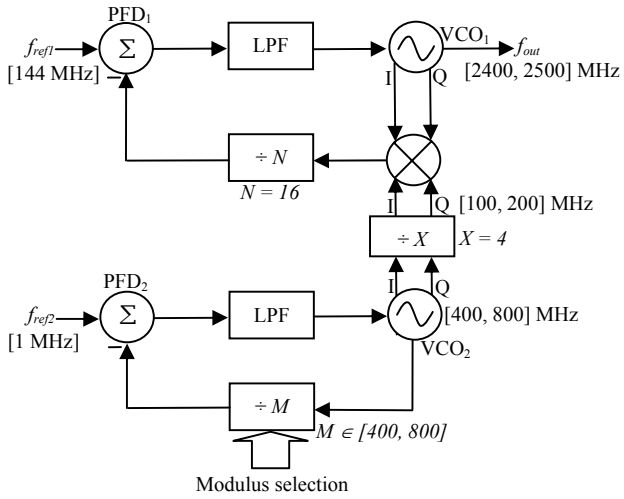

Fig. 6. Concept design and frequency planning of the synthesizer.

The resulting synthesized frequency can be calculated as in (1). This is simply derived by using the result shown in fig. 2.

$$f_{out} = f_{offset} + M\frac{f_{ref2}}{X} = Nf_{ref1} + M\frac{f_{ref2}}{X} \qquad (1)$$

To verify the mathematical feasibility of the design, MATLAB was used. The complete modeling was done on SIMULINK for simplicity. Fig. 7 shows the frequency domain output obtained for a set value on the programmable divider.

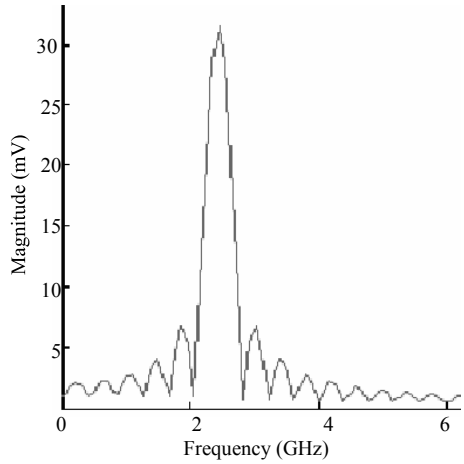

Fig. 7. Spectrum obtained from simulation of the mathematical (SIMULINK) model.

IV. SUBSYSTEMS

The synthesizer was designed by realizing each subsystem at a time. Appropriate input and output loading is used to account for possible loading effects anticipated in the subsystem integration stage of the design. In the next few sections each of the subsystem is discussed.

A. Phase frequency detector (PFD)

PLL performance characteristics may vary depending on the type of phase detector (PD) used. As discussed in [4], several types exist, for high speed performance dual D flip-flop PD is preferred. The PFD may usually contain a charge pump as an integral part of the device. The basic PFD is shown in fig. 8.

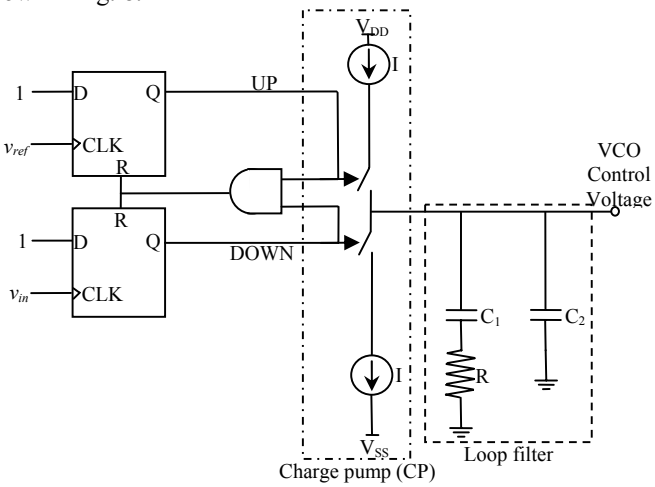

Fig. 8. A PFD with a charge pump output stage.

B. Fixed frequency dividers (÷ N and ÷ X)

Depending on the frequency and the amplitude of the input signals, different types of single-ended or differential

structures for frequency dividers can be chosen. Fig. 9 shows the block diagram of the divide-by-16 *N*-prescalar. The divide-by-4 *X*-prescalar is implemented using the same configuration as the ÷ 4 block of the divide-by-16 *N*-prescalar.

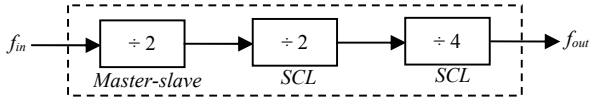

Fig. 9. The divide-by-16 *N*-prescaler.

The Master-slave configuration is a basic Johnson counter. It is implemented as the first stage of the circuit since it can operate with much higher frequencies than source coupled logic (SCL) dividers. A full speed SCL latch is used to implement the ÷2 stage. The configuration [5] is shown in fig. 10.

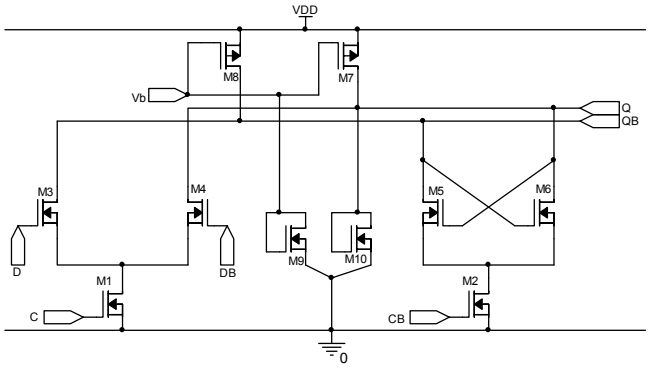

Fig. 10. A full-speed SCL latch.

C. Programmable counter

The counter employs the conventional design [3], which consists of a dual-modulus prescaler (DMP), a pulse (*P*) and a swallow (*S*) counter. At initial reset state, the prescaler divides by (*N* + 1) until the swallow counter overflows, changing the modulus control signal. The prescaler then divides by *N* until the pulse counter reaches *P* counts.

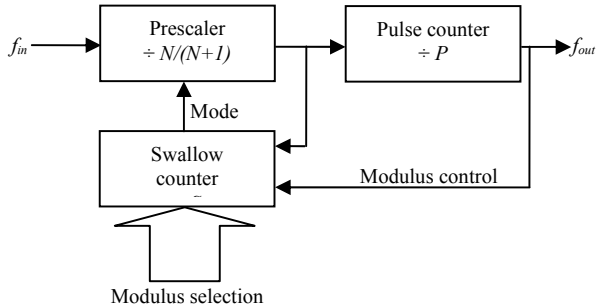

Fig. 11. Block diagram of the programmable divider.

The total counting number M is given by (2).

$$M = P \times \left[(N+1) \times \frac{S}{P} + N \times \frac{P-S}{P} \right] = P.N + S \qquad (2)$$

D. SSB mixer

In the upper-loop, a SSB mixer is needed to obtain the desired sideband for the high frequency prescalar output. Several methods are proposed to design a mixer [4]. The simplest method of achieving SSB is to implement a double side band (DSB) mixer using a Gilbert cell implementation. Thereafter, one of the bands can be filtered to obtain the desired frequency component. However, the DSB-filter configuration is not always practical as the frequency components in this design, viz. (f_1 - f_2) and (f_1 + f_2) are way too close, hence a very sharp filter would be required, which would mean many more resistor and capacitor components. For the synthesizer discussed in this paper, an alternative implementation was done. An I/Q modulator configuration, shown in fig. 12, is used to achieve the required sideband. The I/Q modulator requires both in-and quadrature-phases at its inputs, this poses additional design challenges on the two VCOs which will be required to generate these phases. The DSB units are still implemented using Gilbert cells. Depending on whether the output of the DSB units is being summed or differenced, either the upper side band (USB) or lower side band (LSB) may be obtained.

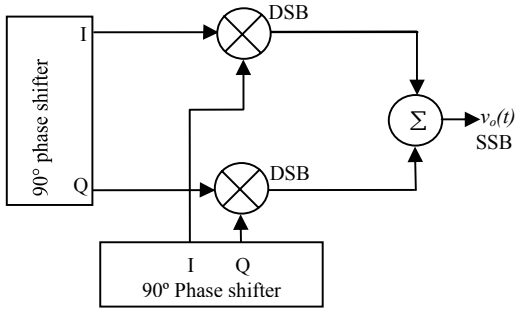

Fig. 12. Block diagram of the SSB mixer.

E. VCO_1: LC oscillator

In order to achieve the phase noise specification for the synthesizer, the high frequency oscillator should have a very good phase noise performance. As indicated in fig. 6, the tuning range is not too wide; hence a good quality LC oscillator suffices. The quality factor, *Q*, of the LC oscillator is basically dictated by the type of inductor used [3]. The type of an inductor used for the synthesizer discussed in this paper is basically the standard spiral inductor as shown in fig. 13.

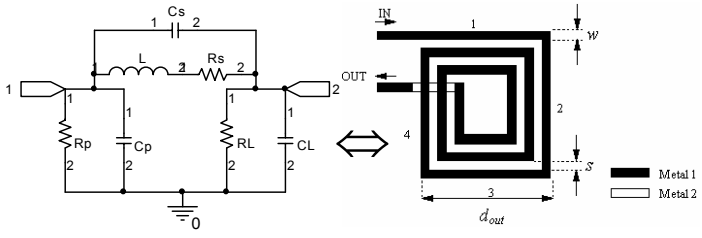

Fig. 13. Simplified model and layout of the inductor.

The inductor was designed using the techniques and software given in [5], [6]. The software (in addition to the geometry parameters) also approximates values for the schematic model of fig. 13, as indicated in Table I.

TABLE I
PARAMETERS OBTAINED FROM THE SPIRAL INDUCTOR DESIGN PROGRAM

Simplified inductor model parameters		Geometry model	
L	3.14 nH	n	3
R_s	6.5 Ω	d_{out}	300 µm
C_L	0.3 pF	w	23.2 µm
R_L,R_P	332 Ω	s	18.1 µm

Simulation was done to further compare the performance of an ideal inductor to spiral on-chip inductor. From these results, the spiral inductor Q was obtained to be about 5.

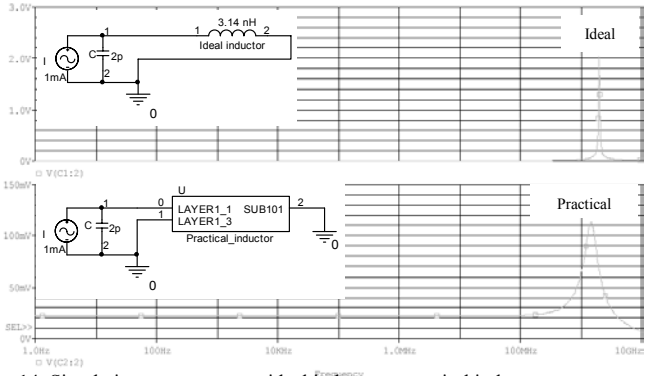

Fig. 14. Simulation to compare an ideal inductor to a spiral inductor.

To complete the tank, a variable capacitor is also required. Several methods exist to implement a varactor [3], the PN junction varactor was used in this synthesizer for simplicity. It consists of a P^+ and an N^+ region residing in an N-well. The depletion region is formed between the P^+ region and N-well. The tuning range provided by a PN junction varactor varies with the doping profile. The PN junction varactor provides a ±10% tuning range.The basic model and layout of the varactor used in the synthesizer discussed in this paper is shown in fig. 15.

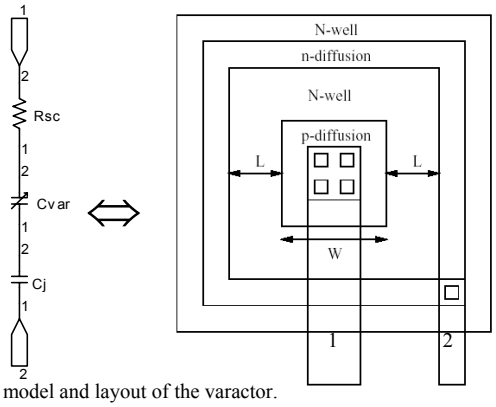

Fig. 15. Basic model and layout of the varactor.

Coupled LC oscillators are known to provide good performance in terms of phase noise, signal amplitude, power consumption, and quadrature output signals [7]. However, IQ amplitude and phase mismatches in these oscillators can be quite large due to the serious mismatch problem of large area inductors and varactors. A simple design modification (as in fig. 16) of the coupled LC oscillators shows a significant improvement of the amplitude and phase mismatches [8].

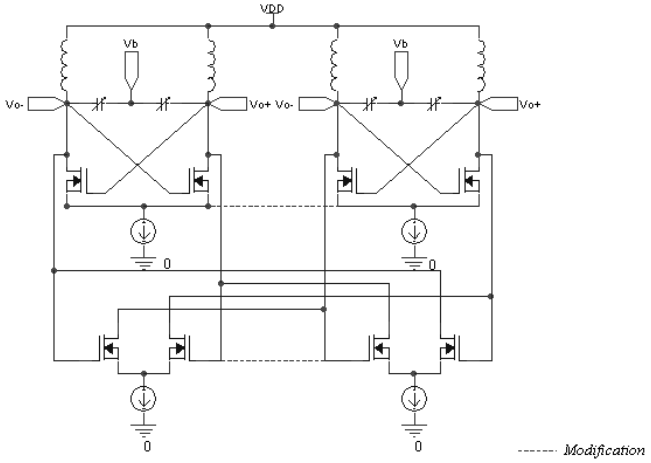

Fig. 16. Coupled LC oscillators with quadrature outputs

Simulation result as shown in fig. 17 from the configuration of fig. 16 confirms that both in- and quadrature phases are achievable.

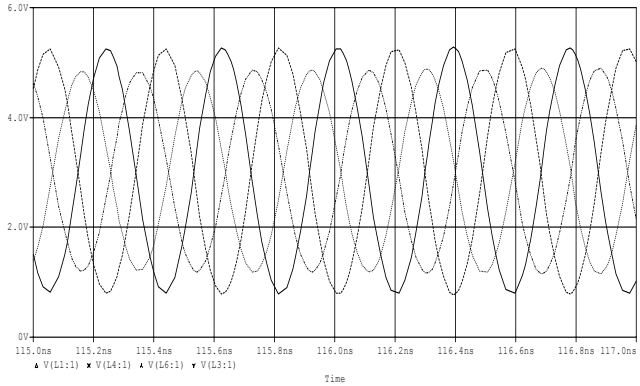

Fig. 17. Time domain simulation result from the LC oscillator circuit.

F. VCO_2: Ring oscillator

The requirements of the lower-loop oscillator are having the centre frequency of 600 MHz and a tuning range around 400 MHz with tuning voltage ranging from 0 to 3.3 V. The phase noise should be smaller than –110 dBc/Hz at 1 MHz offset from the carrier. In order to obtain such a large tuning range, a ring oscillator is used instead of a LC tank oscillator, which has a typical frequency-tuning range limited to around 10-20 % [1]. The feasibility of low noise CMOS ring oscillator that can be comparable with the performance of monolithic LC oscillators has been proven [9]. In this section, the design of a ring oscillator using negative delay path with normal delay path to achieve low phase noise performance is accomplished [10]. The delay cell is designed to have large tuning ability and to achieve constant phase noise as well as constant output signal amplitude throughout the tuning range.

The oscillator is similar to the conventional four-stage ring oscillator (shown in fig. 18) with the exception of a negative delay path. Negative skewed delay path (as in fig. 19) is employed with the normal delay path to obtain higher frequency operation and enhance the tuning range [1].

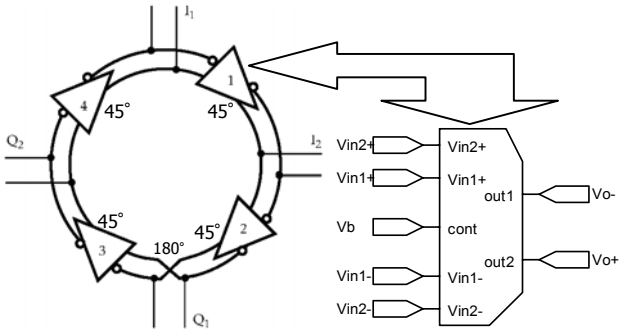

Fig. 18. Block diagram of a conventional four-stage ring oscillator.

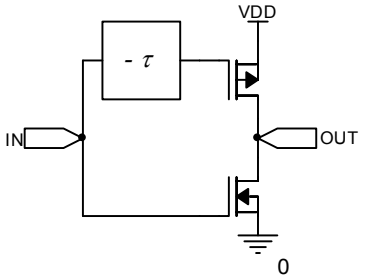

Fig. 19. Conceptual diagram of the negative delay skew idea.

In a conventional differential ring oscillator, the oscillation frequency is limited by the number of delay cells and the unit delay time of a delay cell. The oscillation frequency can be approximated as $1/(2N\tau)$ [1], where N is the number of stages and τ is the delay of the unit delay cell. To increase the operation frequency, the negative skewed delay path is used. With the negative skewed delay path, according to [10], the operation frequency of the oscillator is almost double the value of $1/(2N\tau)$. Simulation results, as shown in fig. 20 confirm this result.

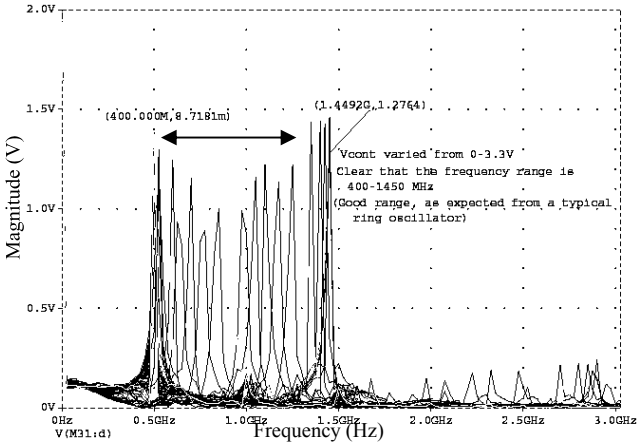

Fig. 20. Simulation result obtained by doing a dc voltage (VCO control) parametric sweep on the ring oscillator circuit.

G. Loop filter

A simple low pass filter is used for this purpose. The basic schematic is shown in fig. 8. A passive implementation is used as it suffices the basic filtering purpose and also saves power.

V. SIMULATION RESULTS

Simulation results of the complete synthesizer are shown in Table II.

TABLE II
CMOS SYNTHESIZER SIMULATION RESULTS

Specification	Theory/aim	Achieved
Frequency range	2.4 – 2.5 GHz	2.4 – 2.5 GHz
Resolution	at least 1 MHz	1 MHz
Phase noise (offset of 10 kHz)	< -80 dBc/Hz	≅ -83 dBc/Hz
Sidebands	about -60 dBc	≅ -60 dBc
Switching time	< 1ms	≅ 30 µs
Power supply	3.3 V, < 60 mA	3.3 V, ≅ 30 mA
CMOS process	Austria Microsystems (AMS) 0.35 µm	

VI. CONCLUSION

A 2.4 GHz fully integrated CMOS PLL frequency synthesizer was designed and implemented. Designing fully integrated frequency synthesizers for wireless systems is always desirable but most challenging. The dual (series) loop architecture was used to obtain more optimal trade-off among phase noise, channel spacing, reference frequency and settling time compared to the conventional integer-N PLL architectures. Furthermore, the use of the improved LC [6], [7] and ring [1], [9] VCO showed, among others, improved phase-noise and spurious-tone performance.

VII. REFERENCES

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