Validation of real-time simulation model of a three-phase Active-Front-End (AFE) rectifier

Presented by:

MD Moshiur Rahman Chowdhury
Budapest University of Technology and Economics
Faculty of Electrical Engineering and Informatics
Department of Automation and Applied Informatics

Outline

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- Code Generation
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- Conclusion & Future work

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Introduction

- In recent years, the demand for the efficient power converters has increased rapidly.
- So, both the converter topology and its control becomes more complex to enhance the quality of power conversion.
- Testing these power converters is a difficult task.
- Conventual tests are very dangerous and time-consuming.
- Hardware-In-The-Loop (HIL) simulation is the desired solution.

Why HIL Simulation

- Industry is constantly developing products
- Those products require designing & testing
- Modeling and Simulation lower development cost and improve the performance
- Possible to inject different failure condition & uncertainties.

Real-Time Simulation Models Active-Front end (AFE) rectifier

- An active front end (AFE) drive replaces the diodes in the rectifier with IGBTs, which significantly reduce harmonics and allow regenerated power to be fed back to the supply.
- IGBTs are devices whose switching is controlled electronically — hence the term “active” front end.
- The active front end monitors the input current waveform and shapes it to be sinusoidal, reducing total harmonic distortion (THD) to 5 percent or less.

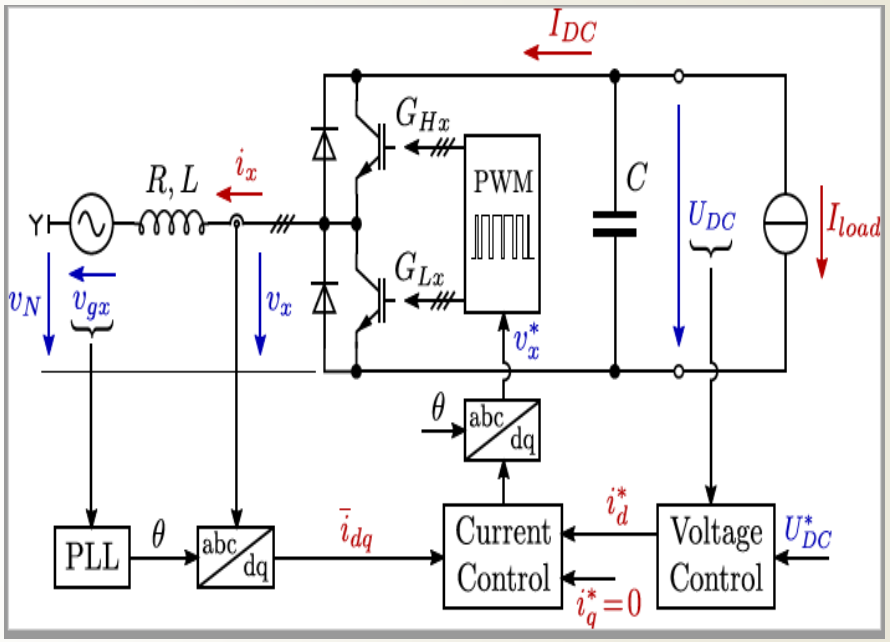
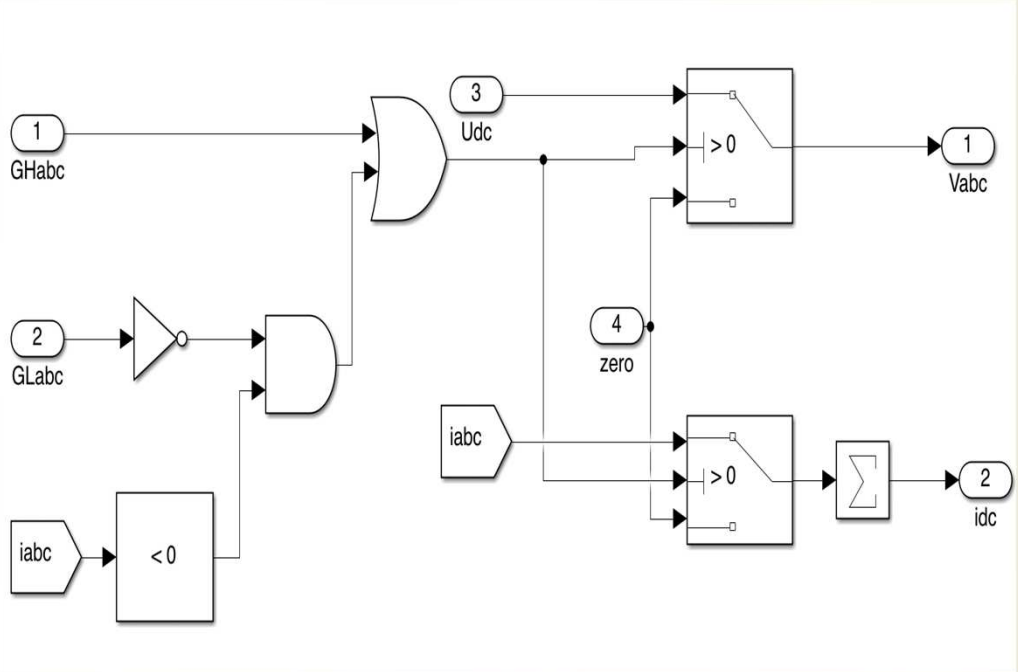


Fig. Three-phase Active Front-End (AFE) rectifier.

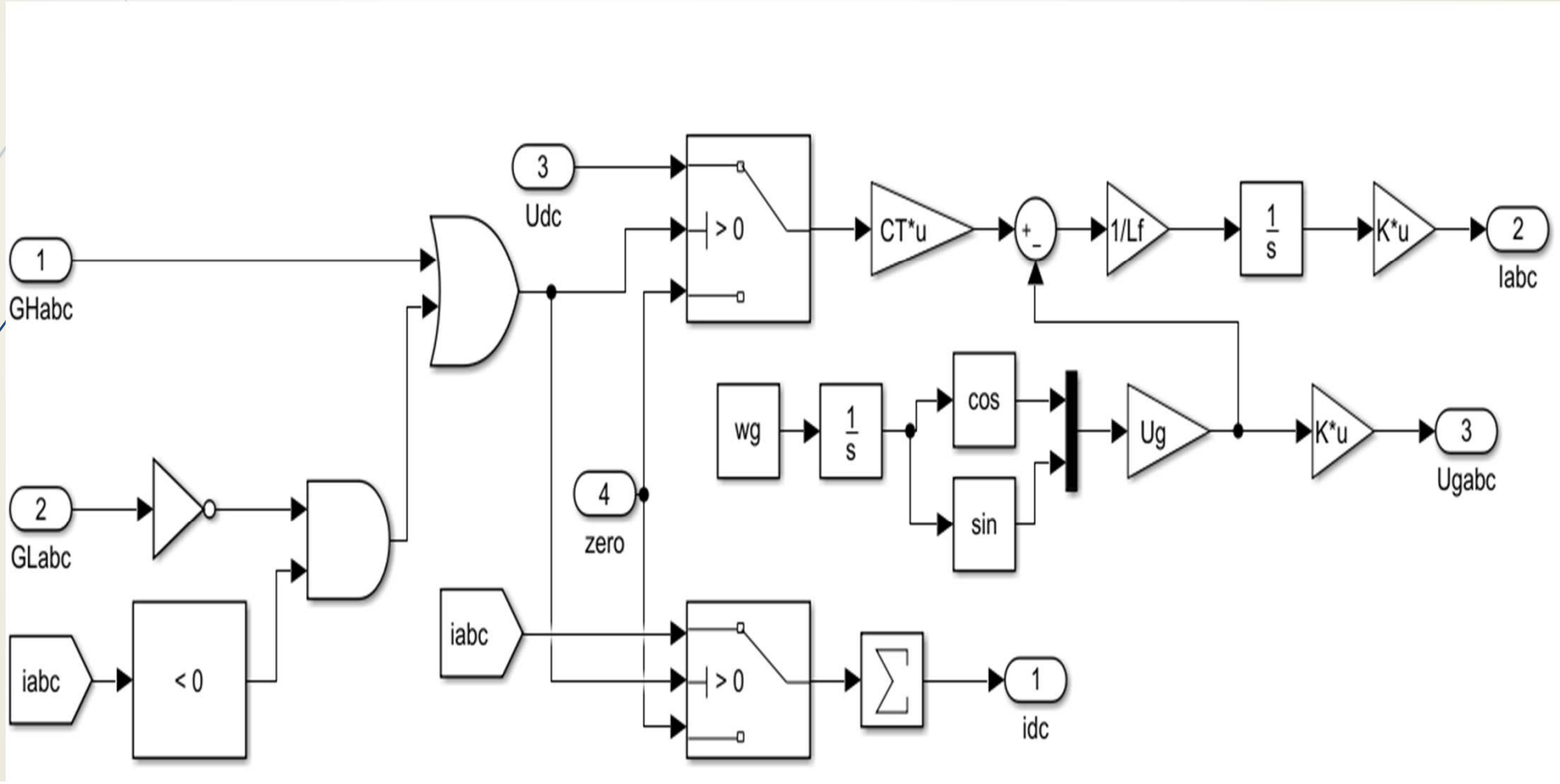
Switching logic of the half bridge arm

SWITCHING LOGIC OF A HALF-BRIDGE ARM.

G_{Hx}	G_{Lx}	i_x	v_x	I_{DCx}
1	0	$\times$	U_{DC}	i_x
0	1	$\times$	0	0
0	0	<0	U_{DC}	i_x
0	0	>0	0	0
1	1	Short Circuit		



Simulink model of rectifier bridge with choke



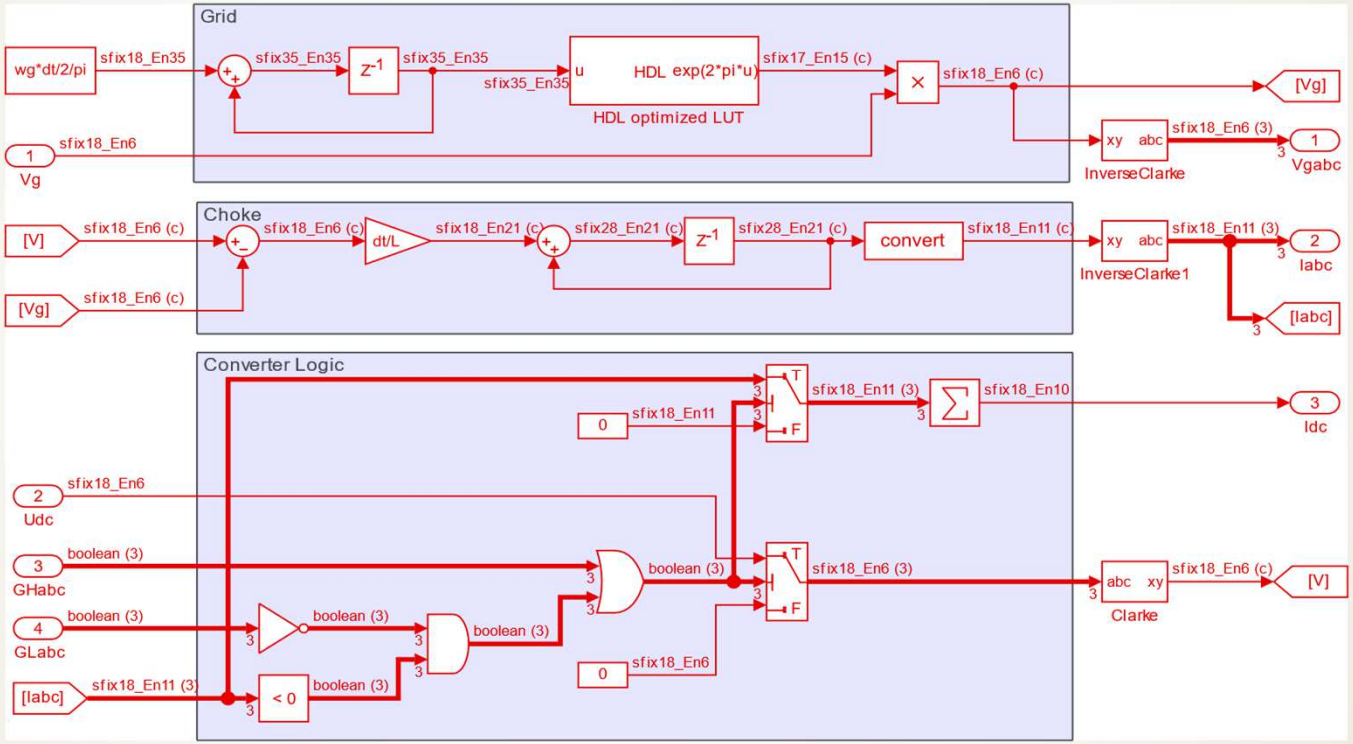
Design Parameters

Main parameters used for the AFE model

Name	Value
Grid peak phase voltage V_g	325 V
Grid frequency f_g	50 Hz
Choke inductance L	1 mH
Switching frequency f_{sw}	10 kHz
DC bus voltage U_{dc}	700 V

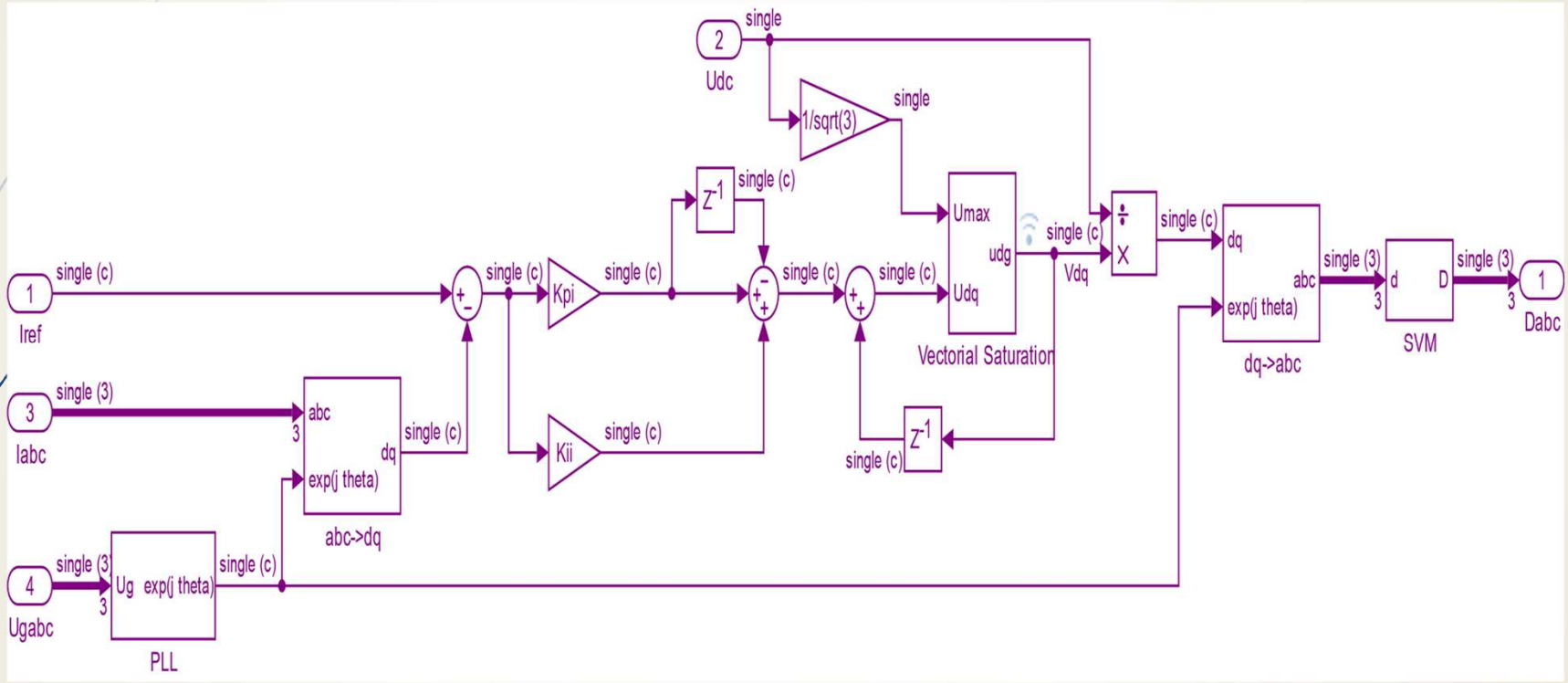
Code Generation for FPGA

Simulink model of the grid, the choke and the rectifier bridge used in the HDL code generation for the FPGA

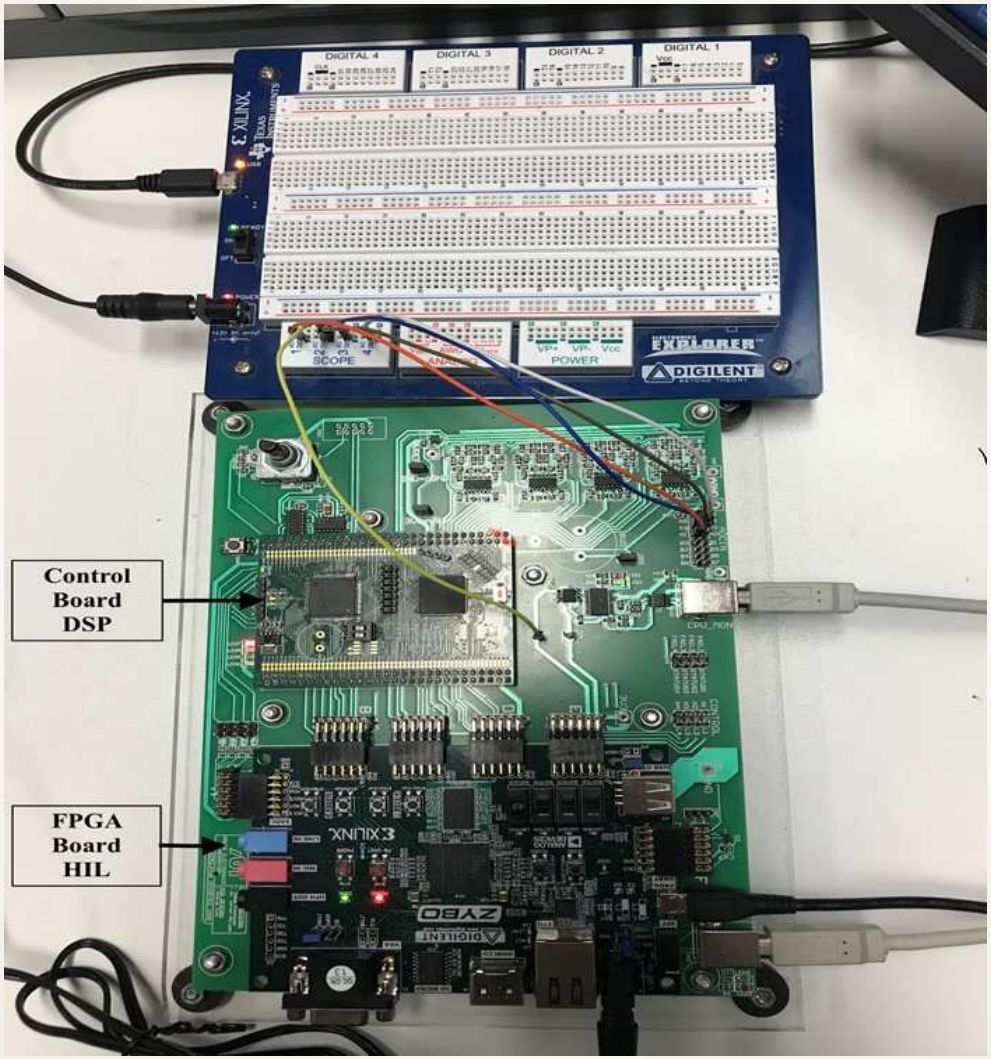


Current Control Model

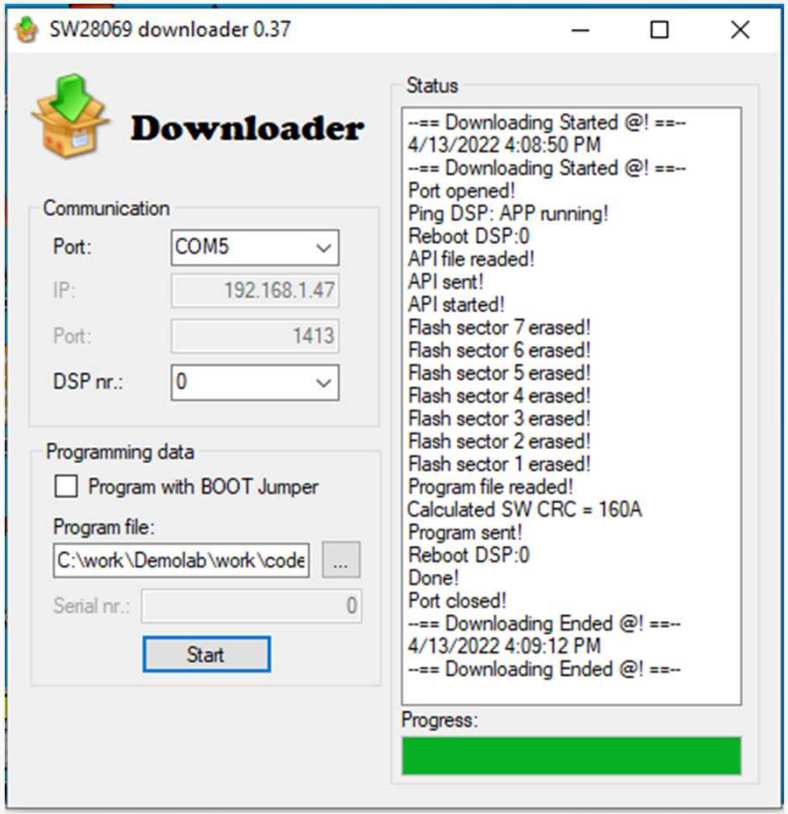
Current control Simulink model used in C code generation for the DSP



The HIL hardware with Digilent Zybo board

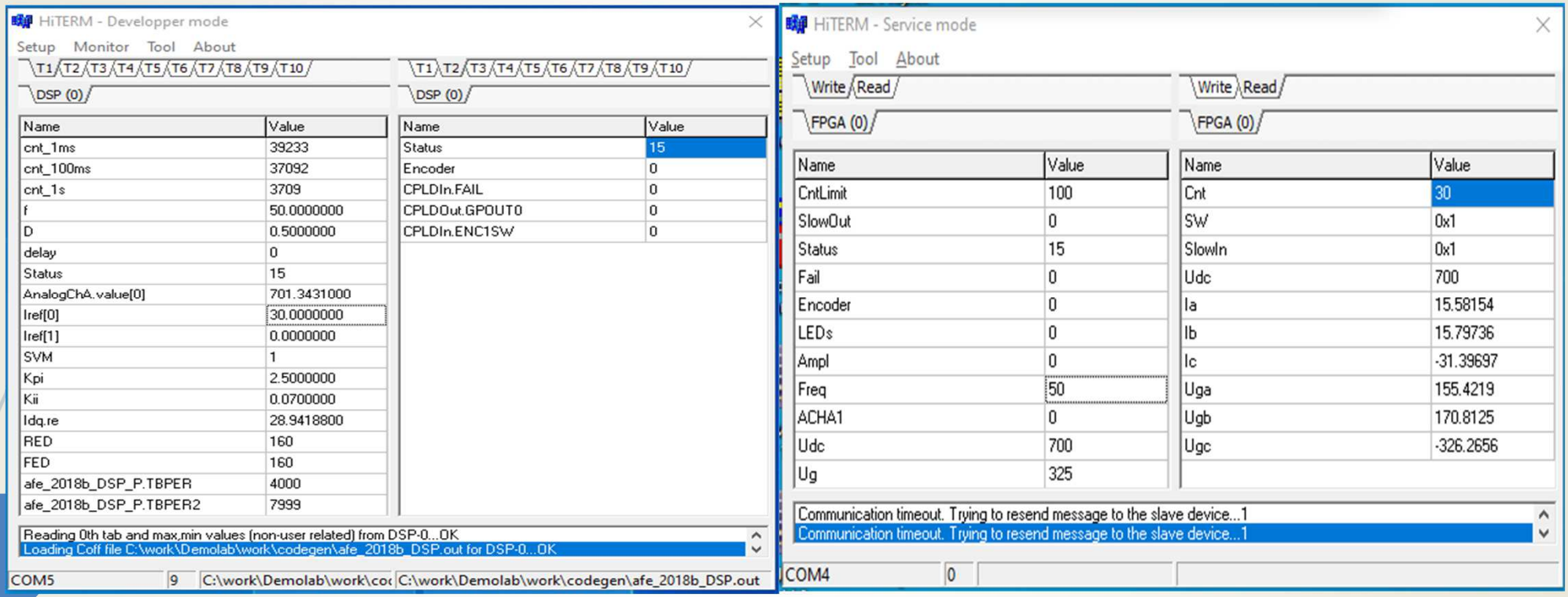


Terminal Program Interface



Programming software tool for DSP

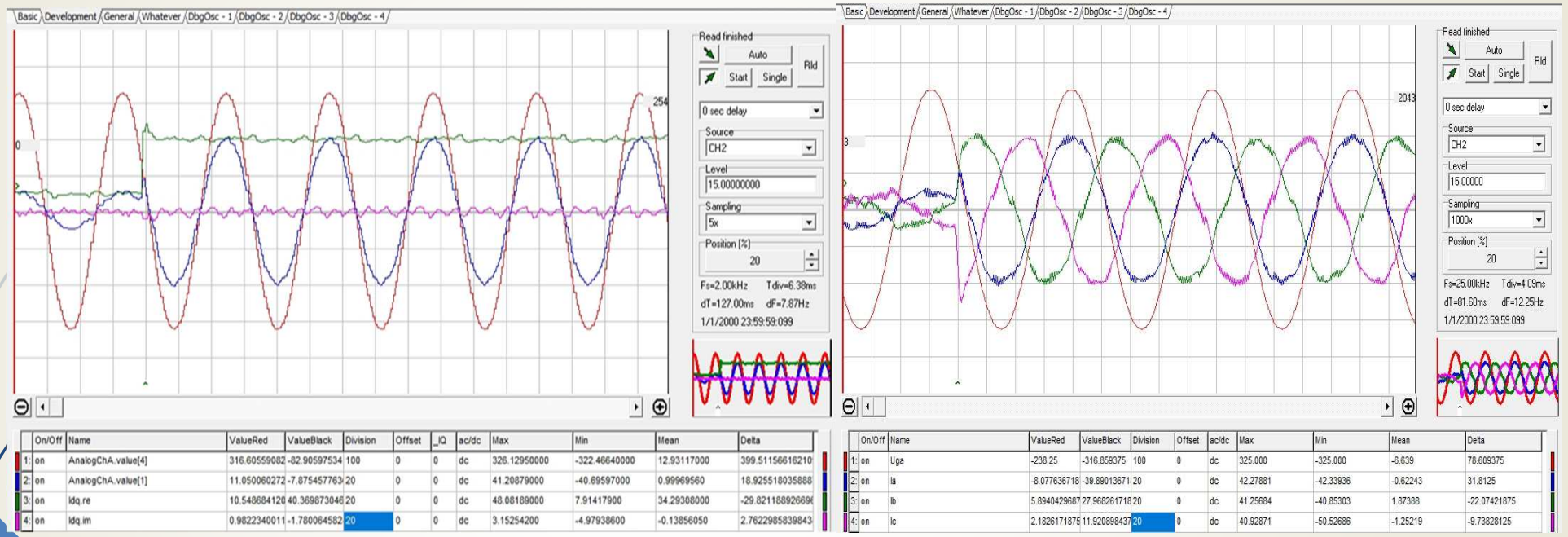
Terminal Program Interface



(a) **(b)**

Interface for DSP side (a) and FPGA side (b)

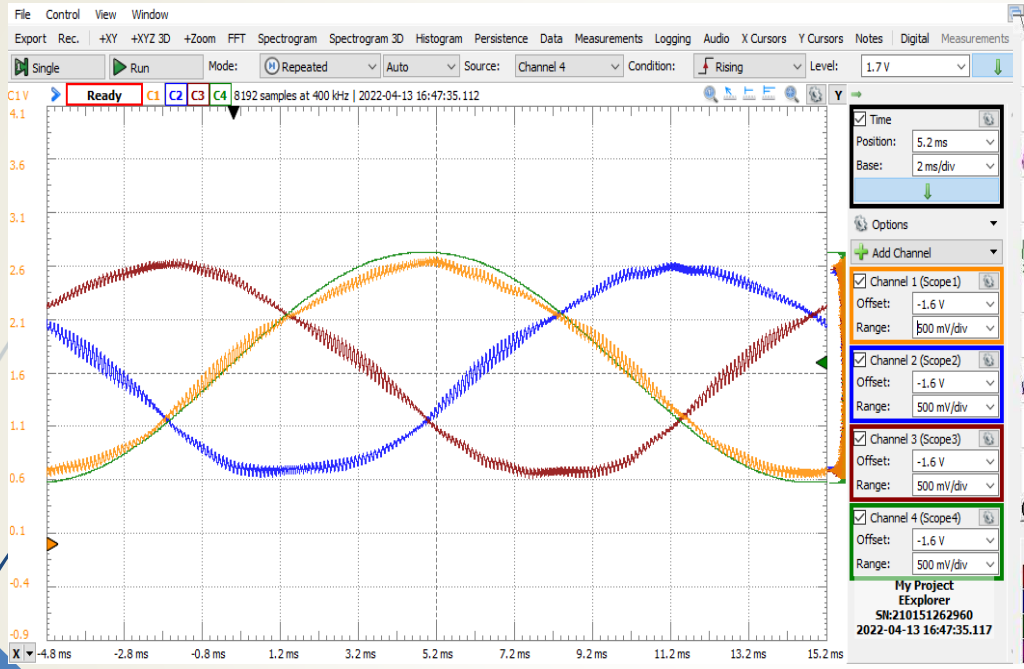
Simulation Result



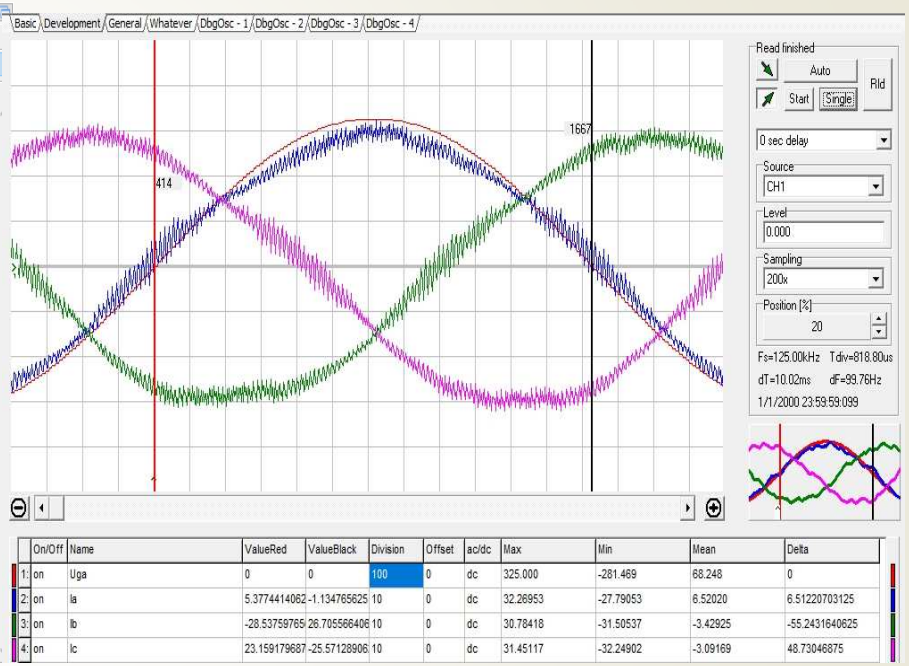
(a) **(b)**

Current from DSP side (a) and FPGA side (b) with deadtime 2µsec whereas d reference current steps from 10A to 40A

Simulation Result Cont.



(a)

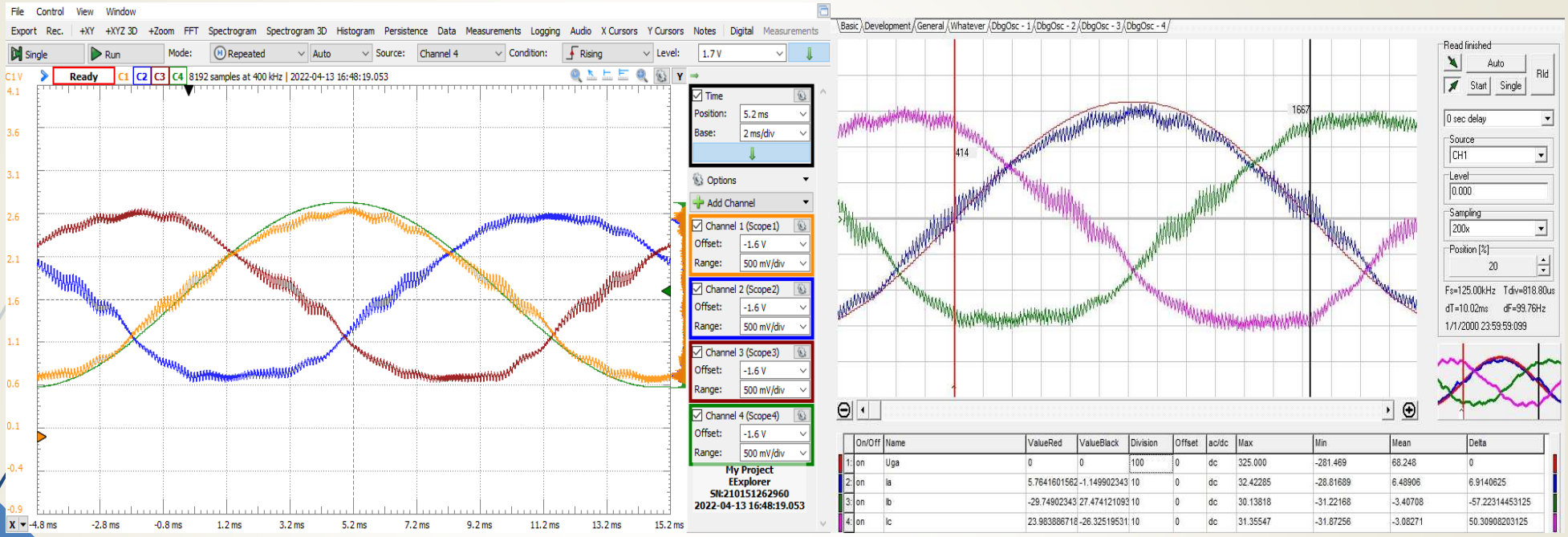


	On/Off	Name	ValueRed	ValueBlack	Division	Offset	ac/dc	Max	Min	Mean	Delta
1:	on	Uga	0	0	100	0	dc	325.000	-281.469	68.248	0
2:	on	Ia	5.3774414062	-1.134765625	10	0	dc	32.26953	-27.79053	6.52020	6.51220703125
3:	on	Ib	-28.53759765	26.705566406	10	0	dc	30.78418	-31.50537	-3.42925	-55.2431640625
4:	on	Ic	23.159179687	-25.57128906	10	0	dc	31.45117	-32.24902	-3.09169	48.73046875

(b)

Three-phase current time function where the d direction reference current is 30A with deadtime 0 µsec from the 4-channel scope (a), from the FPGA side (b)

Simulation Result Cont.



(a) **(b)**

Three-phase current time function where the d direction reference current is 30A with deadtime 2 µsec from the 4-channel scope (a), from the FPGA side (b)

Conclusion & Future work

- The HIL simulation framework has been developed for real-time testing of the AFE rectifier control algorithms
- The system exhibited realistic behaviors
- The control model can be extended
- A non-ideal grid model with a grid impedance and harmonics to create more realistic behaviors in the HIL system.


Thank
you