For IEEE LM Newsletter

75th anniversary of the transistor at EPFL Neuchâtel, March 30th, 2023

At the invitation of the IEEE Solid-State Circuits Chapter of Switzerland, a commemorative and networking event was held at the EPFL Microcity building in Neuchâtel. In the first part of the afternoon, we had the honor to host three Distinguished Lecturers (Fig. 1).

Prof. Tom Lee presentation "*From Rocks to Chips: Stories of the Transistor*" covered the early history of the transistor. Then, Dr. Chris Mangelsdorf described circuit design techniques using the bipolar junction transistor (BJT) in his talk "*Don't Try This With CMOS!*". Finally, Prof. Christian Enz concluded this session describing the development of low power CMOS using the EKV MOSFET model.

The second part of the afternoon, "*From transistor manufacturing in the late 1950's until today*" hosted five speakers who were key actors or are still active in the semiconductor sector of Switzerland.

Hugo Wyss, IEEE Life Senio Member, went back to the earliest beginning of Transistor manufacturing technology in Switzerland, taking place at ETHZ/AFIF (Prof. E. Baumann) in 1956, where Dr. A. Müller established the first germanium junction alloy transistor manufacturing line, thanks to a license agreement that Hasler Werke Foundation closed with Western Electric (Jack Morton) and Bell Labs in 1952. Some research on Ge Transistor done at L.S.R.H. in Neuchatel induced then Ebauches SA to also start manufacturing of Ge alloy transistors under a sublicense of Philips Gloelampen, Netherlands by the early 1960 in Neuchatel. Such transistors being used for the „Dynotron" electrical watch movements competing with those of LIP France.

By 1963 there were two Ge transistors manufacturing lines in Neuchatel, since the pilot line of ETHZ was transferred to FAVAG Neuchatel and expanded to a mass production of the famous HT101 transistors, which enjoyed long life at Hasler AG, Bern, as components for phone and telex exchange centrals. Ebauches SA gave up production of transistors by 1970, since silicon was making inroads and was also picked up by FAVAG, where Hugo under the leadership of Dr.Müller started manufacturing them by 1968.

But, already by 1965 at Centre Electronique Horloger SA (CEH), founded and started 1961 by Dr.Roger Wellinger (1919-2014), a state of the art silicon wafer fab was set up and run by Dr. Kurt Huebner, an alumnus together with Adolf Goetzberger of Bill Shockley in Mountain View (1958-1962). Huebner produced the first monolithic silicon IC as electronic circuit driving an Accutron-like H-shaped metallic resonator, whose frequency was nearly independent from gravity (Alpha-Project). All subsequent bipolar ICs become increasingly complex, and the technology was later licensed to FASELEC AG in Zurich, a Philips subsidiary.

So, Neuchatel became the Swiss semiconductor hub and is still today, with CSEM and EM Microelectronic in Marin. As usual with very innovative projects, the success of CEH with the development of the first quartz electronic wristwatch incorporating a silicon IC (an IEEE Milestone) didn't help the career of its founder Roger Wellinger, who was summarily fired in 1968 and then went over to other activities, becoming IEEE Region 8 Director 1969-1970 and promoter of the first European IEEE Conference EUROCON 1971 in Lausanne. His son John, attending the commemoration, gave a short overview of his father's curriculum, who immigrated to the US as a post-doc in 1946.

Prof. Eric Vittoz, Life Fellow Member, presented his constant quest for low power electronics, which started with a 10 microamp quartz clock demonstrator using BJTs in 1962 (Fig. 1), opening the route for the quartz wristwatch. Bipolar integrated circuit were part of the CEH Beta1 watch prototype of 1967 and the Beta21 watch (Fig. 3).

Already in 1968, Eric designed a Low-Voltage CMOS Divider in an experimental Metal-gate CMOS technology developed at CEH by Fritz Leuenberger. An invited paper was published in the IEEE Proceeding in Sep. 1969. The concept of digital tuning of the quartz introduced in 1971 on a CMOS LSI with 500 transistors, is now standard practice in watches with on-chip EEPROM. Improved frequency dividers in a new 5 micrometer CMOS technology were published in the IEEE Journal of Solid-State Circuits in 1972.

His discovery of the exponential characteristics Subthreshold Weak Inversion in 1967, lead to the implementation of ultralow power CMOS circuits in 1976 and the development of symmetrical MOSFET models for design and simulation, leading the way to the EKV MOSFET model.

With Alain-Serge Porret, CSEM Vice President for Integrated and Wireless Systems, we jumped to the future. Based on many years of low power imagers developments, a circuit was developed to analyze the electrical activity of live brain cells grown on a chip. CSEM also made brain depth electrodes with a specialized Application Specific Integrated Circuits (ASIC), to localize and treat epileptic seizure (Fig. 4). The low-power expertise in imagers, processing and radio communication is the foundation for innovative low power AIoT (Artificial Intelligence of Things). A sub-milliwatt demonstrator (Fig. 5) is using Artificial Intelligence capable to recognize faces and various emotions.

State-of-the-art products designed in Switzerland benefit from the local low power semiconductor expertise. To illustrate it, Evert Dijkstra, recently retired Managing Director of Phonak Communication, Sonova, explained that Application Specific Integrated Circuits (ASICs) contribute to the success of this hearing aid manufacturer. The wireless communication custom chip (Fig. 6) supports up to seven protocols at 2.4 GHz. The 6 mm2, 41 million transistor device operates at 1.2 volt, with a consumption comprised between 1.3 and 3.2 milliwatt, depending on the mode. All their ASICs are designed in cooperation with Swiss based companies or institutions.

The role of Swiss companies in equipments for semiconductor manufacturing is generally less known. André Gerde, CTO of Comet Group demonstrated that their highly accurate RF power for Plasma Control Technology (Fig. 7) is used to produce the most advanced semiconductor wafers. The 75-year-old company produces X-ray tubes since 1948. Today comet builds the X-ray 2D and 3D inspection machines required for the advanced packaging methods (Fig. 8).

This event was attended by many IEEE Life Members, IEEE Members and Students. It concluded with intense networking discussions at the cafeteria.

Header

Fig. 1 EPFL Microcity, Neuchâtel

Fig. 2 CEH Low Power quartz clock demonstrator

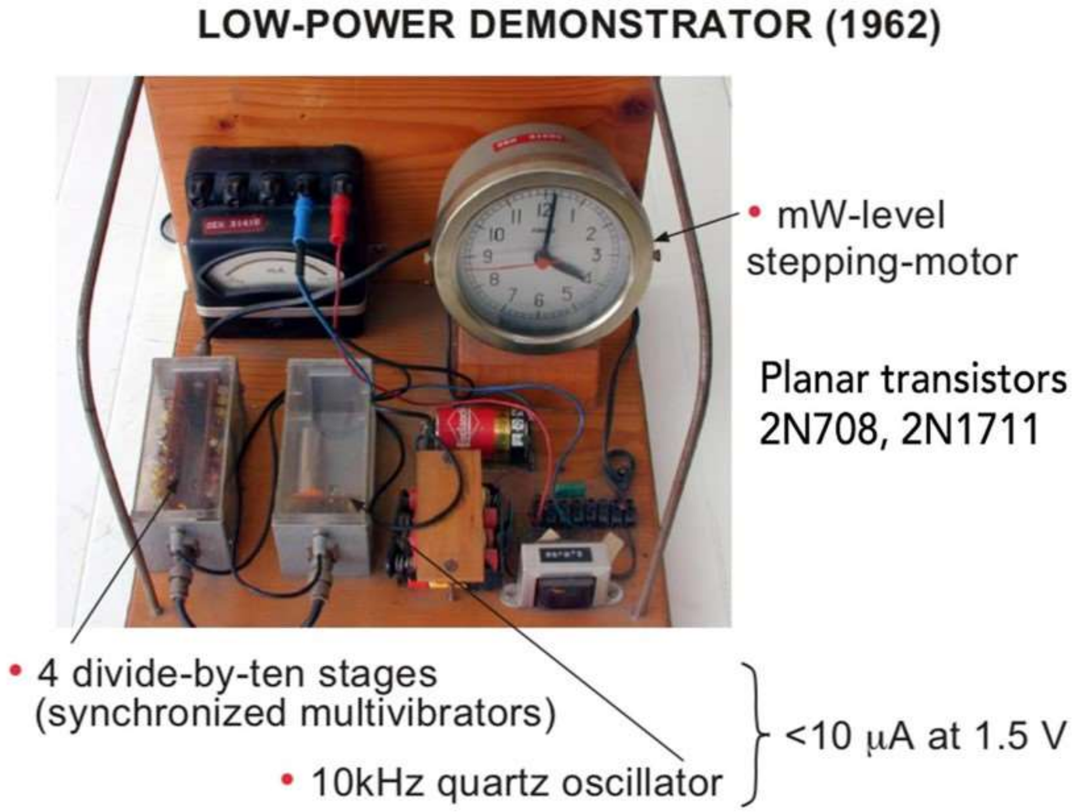

Fig. 3 CEH Bipolar Integrated Circuit

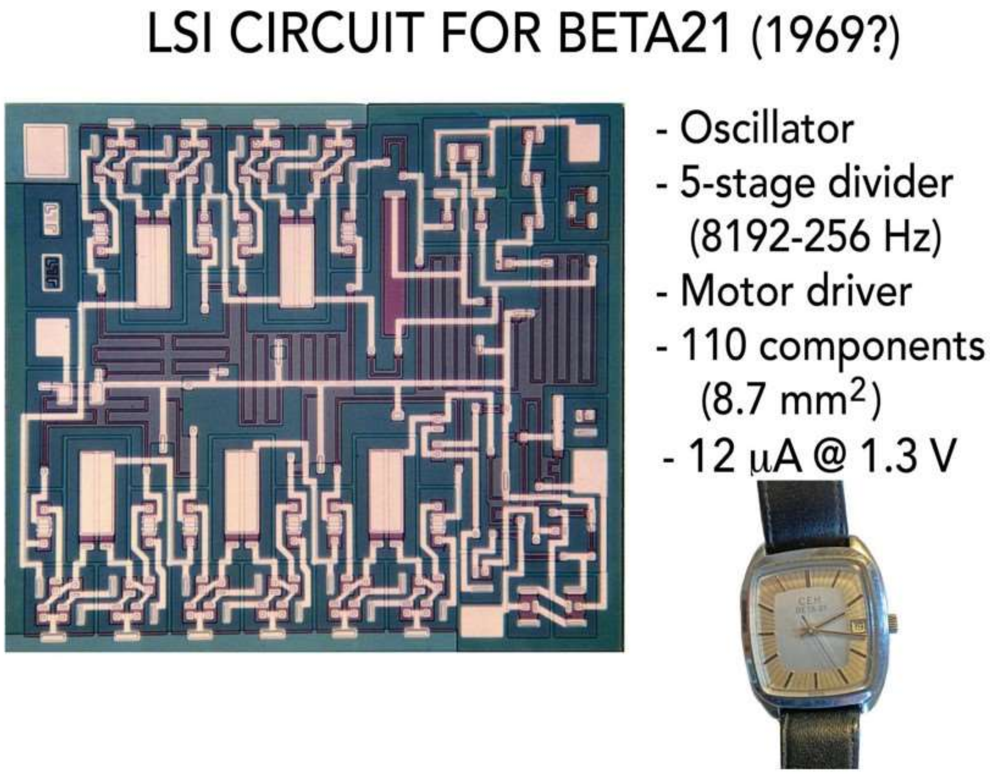

Fig. 4 CSEM ASIC for brain depth electrodes

Fig. 5 CSEM sub-milliwatt Artificial Intelligence demonstrator

Fig. 6 Sonova – Phonak wireless communication custom chip

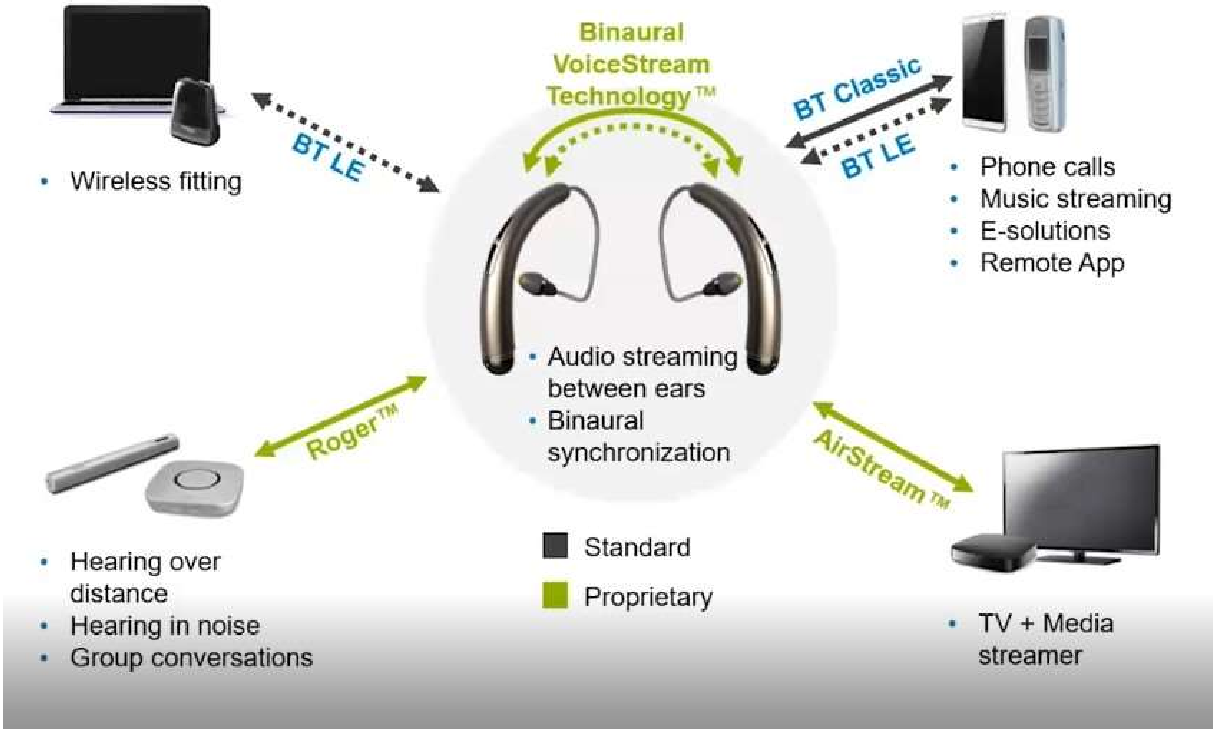

Fig. 7 Comet AG RF power for Plasma Control Technology

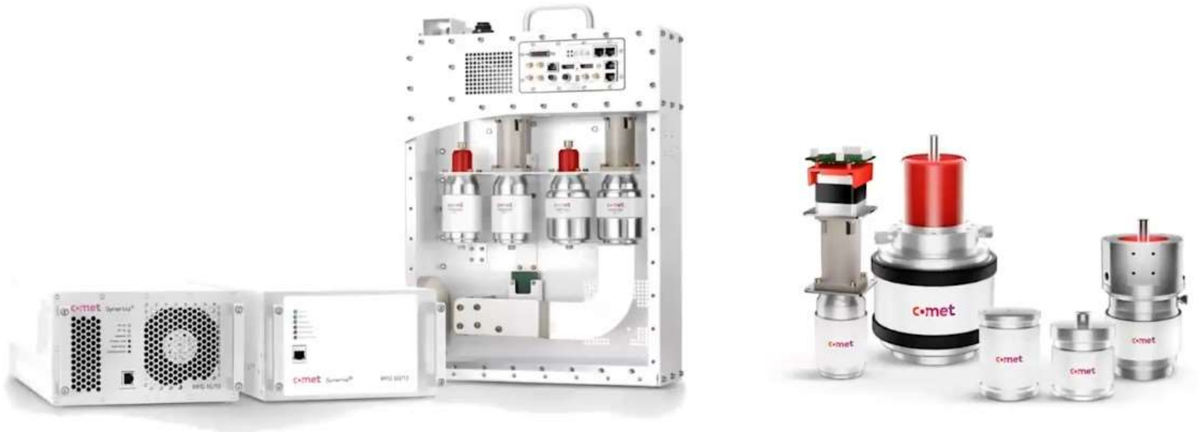

Fig. 8 Comet AG X-ray inspection for advanced packaging