Enhancement of VCO linearity and phase noise by implementing frequency locked loop

***Abstract*— This paper investigates the on-chip implementation of a frequency locked loop (FLL) over a VCO that decreases the phase noise and linearizes the transfer function. Implementation of the FLL inside a PLL is also investigated and a possible application is highlighted. Design of a special kind of low noise frequency detector without a reference frequency (frequency-to-voltage converter), which is the most critical component of the FLL, in a 0.25 μm BiCMOS process is also presented. Linearization and approximately 15 dBc/Hz phase noise suppression is demonstrated over a moderate phase noise LC VCO with a center frequency of 10 GHz.**

I. Introduction

VCOs are one of the most critical blocks in PLLs, so there is a huge research going on to improve the performance of the VCOs. The FLL that includes a VCO, a frequency-to-voltage (f2V) converter, a voltage-to-current converter and the loop filter will be defined as the proposed ”VCO block” in this paper. The advantages of having a FLL around a VCO in a PLL can be summarized as following two points.

VCO is a non-linear device by nature. FLL makes the ”VCO block” tuning curve linear. This brings the advantage of having the same VCO gain for different frequencies inside the VCO tuning range. When the VCO gain changes due to non-linearity, the loop gain of the PLL changes for different frequencies inside the frequency range. This results in a compromise on the jitter transfer of the module. That’s why; using a linear VCO block gives the advantage of having the same jitter transfer in all frequencies inside the frequency range using the same loop filter.

PLL with a low loop bandwidth filters the phase noise in the reference, but can not suppress the phase noise of VCO in frequencies higher than PLL bandwidth. FLL with a high loop bandwidth over the VCO decreases the phase noise of the VCO inside the FLL bandwidth.

The advantage of implementing a FLL over a VCO can be observed in both of the main VCO types. Implementation of FLL can linearize the LC VCOs by relatively decreasing the phase noise, depending on the f2V converter noise contribution. On the other hand, the phase noise of ring oscillators can be decreased extensively by obtaining more linearity. The phase noise performance of the FLL depends mainly on the f2V converter noise, so phase noise of higher noise VCOs can also be decreased to similar amounts with lower phase noise VCOs.

Following application of the FLL can highlight the advantage of this method. In applications using PLLs, there are parts, where output jitter is more critical such as outputs and where it is more relaxed such as inputs. In these kind of applications, a ring oscillator is used when output jitter is not that critical, but low phase noise LC VCOs are used in PLLs, where output jitter is important. That’s why; two different VCOs are implemented. If in the noise critical PLL, FLL is implemented over the same ring oscillator that is used in the input, phase noise of the ring oscillator can be suppressed and frequency locked ring oscillator can be used in the output. This way the control voltage of the ring oscillator in the input can be copied to the other ring oscillator and substantially decrease the locking time. This frequency locked VCO will be linear as well and having the same gain over the frequency range will be another advantage.

Up to our knowledge, there has not been any work published implementing FLL inside a PLL on chip, in order to decrease phase noise and achieve linear control on VCOs. However; there are some works to implement it by discrete components [1]. Use of switched banks in digitally controlled oscillators gives a relative linearity to the oscillator transfer function, which is an active research area both industrially [2] and academically [3], [4]. Main disadvantages of this way of linearization are complexity, extra circuitry, increase in locking time and power consumption. FLL is a good alternative to this method and both can be used together as well.

In this paper, linearization concept will be discussed in section II, followed by phase noise suppression in section III. Transistor level design of a f2V converter, which is the most critical component in the loop, will be explained in this section as well. In section IV, implementation inside a PLL will be explained and feasibility of implementing another loop inside a PLL will be demonstrated.

II. Linearization

A. Linearization concept

The principle of linearizatin can be described as follows. The tuning curve of the proposed ”VCO block”, which now consists of FLL, is independent from the VCO tuning curve and determined by the response of the f2V converter. Once the FLL settles, the output frequency is set by the input voltage, which acts as an offset voltage on the response of f2V converter.

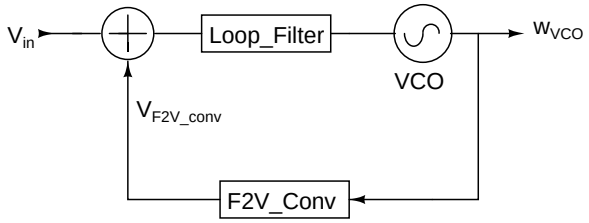

Fig. 1. The proposed "VCO Block" containing FLL

The f2V converter output voltage has to compensate the offset created by the input control voltage and overall transfer function of the system follows the linear transfer function of this component. Hence, the structure can be used as a new VCO, where V_{in} is the control voltage and w_{vco} is the output frequency. The proposed VCO block is shown in Fig. 1.

In order to see how the concept works, let's first look at the equations of the loop. The output voltage of the f2V converter can be defined as (1), where g(x) is the transfer function of the f2V converter.

$$V_{F2Vconv} = g(w_{VCO}) \tag{1}$$

After being subtracted from the overall control voltage of the proposed VCO block (V_{in}) and integrated by the filter, the input voltage of the VCO ($V_{LF_{out}}$), which is the output voltage of the loop filter, is calculated by (2). Here, contribution of the f2V converter is subtracted, so in the actual implementation, it will be designed with a negative slope transfer function. T is the integrator constant of the loop filter.

$$V_{LF_{out}} = \frac{1}{T} \cdot \int (V_{in} - V_{F2Vconv}) \cdot dt \tag{2}$$

By using the information from (2), output frequency of the FLL is written as (3).

$$w_{VCO} = K_{VCO} \cdot \frac{1}{T} \cdot \int (V_{in} - V_{F2Vconv}) \cdot dt \tag{3}$$

When the loop settles, e.g. in the steady state, VCO frequency will not change any more, so when t $\rightarrow \infty$;

$$\frac{\partial w_{VCO}}{\partial t} = \frac{K_{VCO}}{T} \cdot (V_{in} - V_{F2Vconv}) = 0 \tag{4}$$

Using (1) and (4), as K_{VCO} cannot be 0,

$$w_{VCO} = g^{-1}(V_{in}) \tag{5}$$

As it's seen in (5), output frequency of the VCO is now dependent on the inverse function of the f2V converter and independent of the VCO sensitivity variations. The f2V converter is the new master of the loop and center frequency is also set by the f2V converter and not the LC tank of the oscillator.

In order to see the transfer function of f2V converter and how it matches up with these equations to give a linear voltage frequency characteristics for the VCO block, one can refer to section III-A and particularly look at (11). As transfer function of the f2V converter is linear, it can be defined as a constant $K_{F2Vconv}$ instead of a g(x) function, so (5) can be written as;

$$w_{VCO} = \frac{1}{K_{F2Vconv}} \cdot (V_{in}) \tag{6}$$

From (6), it can be seen that the proposed "VCO block" will have a linear transfer function with a constant gain determined by f2V converter.

B. Simulation results

An example using verilog-A models is used in this section to prove the concept. For the simulations, both VCO and f2V converter is set to work at frequencies between 9-11 GHz. For f2V converter, 0.5V and -0.5V corresponds to 9-11 GHz in order to have a reasonable sensitivity value, which is targeted in the application, so the input control voltage should be swept between -0.5V and 0.5V in order to move along the full f2V converter response.

The working principle of the system can be described as follows. When the FLL is settled, for example at the center frequency, the control voltage and output of f2V converter will add up to zero and oscillator output frequency will not change anymore. When a positive offset voltage is applied as the input control voltage, the voltage of the output of adder will increase and after integration, this will result in an increase in the output frequency of the oscillator. This increase will be detected by the f2V converter and will be converted as a negative voltage corresponding to that frequency, because of the negative slope sensitivity. This way, the loop will stabilize again, when the input voltage of the integrator adds up to zero. So the new output frequency will correspond to another voltage-frequency point in the response of the f2V converter, which becomes the master of the loop. The steps explained can be followed in Fig. 2.

In Fig. 2, first graph is the external control voltage, second graph is the corresponding frequency detector output voltage, 'third graph shows the output voltage of the adder, fourth graph is the output of the integrator and last graph is the output frequency of the proposed

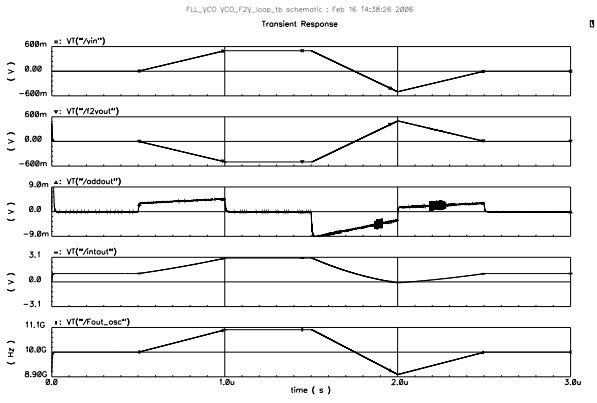

Fig. 2. The linear response of the "VCO block" to all kind of input control voltage transitions

”VCO block”.

The comparison between the standalone VCO having a square root transfer function and the same VCO inside the FLL, which constitutes frequency locked VCO (FLVCO), is done by applying the same input voltages to both and looking at the output frequencies. Input voltage of 0V to 3V is applied to both of the systems and a divider and offset circuitry is placed in front of the ”VCO block” to get the required voltage range in the input. The voltage-to-frequency responses and the derivatives of the responses are seen in Fig. 3. It’s seen on the left that a square root function can be converted to a linear transfer function and on the right the slope of the ”VCO Block” transfer function is constant over the input voltage range as desired.

III. Phase Noise Suppression

It’s much faster to run phase noise simulations on phase domain models, because high frequency variations associated with the voltage-domain models are not present in phase-domain models. These models are suitable for phase noise simulations, so all components in the design are modeled in phase domain. Noise contributions of the individual component is added to the models and overall phase noise of the system is simulated.

In order to see the phase noise suppression of the FLL, it’s required to see the noise contribution from the f2V converter, which becomes the new master of the loop, also in terms of noise contribution, which will be evident with equations in section III-B.

A. Transistor level design of f2V converter

After investigating several f2V converter topologies, dual slope detector is found to be the most suitable, in terms of low noise, acceptable detector gain within an acceptable frequency range and high speed.

Slope detectors are the simplest type of frequency detectors. In spite of its simplicity, the slope detector is rarely used because it has poor linearity. It is necessary to look at the expression for the voltage across the LC tank in the slope detector, in order to understand why this is the case. Resonant frequency of the LC tank is

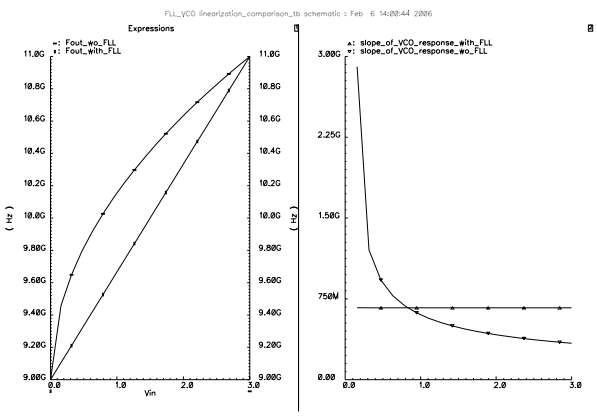

Fig. 3. a.Sensitivity of VCO and FLVCO b.Derivative of sensitivity

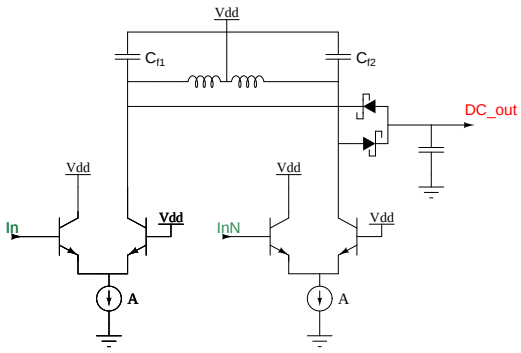

Fig. 4. Dual slope f2V converter schematic

defined as: $w_0 = \frac{1}{\sqrt{LC}}$, so the voltage of the LC tank is;

$$V_{LC} = I_{LC} \cdot (\frac{w_{in}^2 - w_0^2}{w_{in}}) \cdot L \tag{7}$$

Since the frequency deviation of the FM signal is directly proportional to the modulating signal’s amplitude, the output of the slope detector will be distorted, because output voltage is not directly proportional to frequency deviation in (7).

Because of the poor linearity of single slope detectors, a dual slope detector is designed as shown in Fig. 4. Two LC tanks are designed and resonance frequencies are set to approximately 9 GHz and 12 GHz in order to cover the center frequency and required frequency range and give a detector gain of acceptable value. The outputs of this two slope detectors have opposite signs because of the way they are connected to the amplitude detectors and are subtracted from each other. This results in a linear region in between two frequencies as seen in Fig. 5.

In order to see how this circuit works, one can write the output voltage of the f2V converter as in (8), assuming contribution from parasitic resistances cancel each other in subtraction;

$$V(out) \approx \frac{w_{0f2}^2 - w_{0f1}^2}{w_{in}} \cdot L \cdot I_{LC} \tag{8}$$

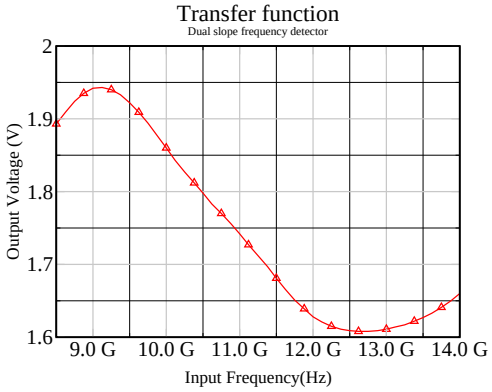

Fig. 5. Transfer function of dual slope f2V converter

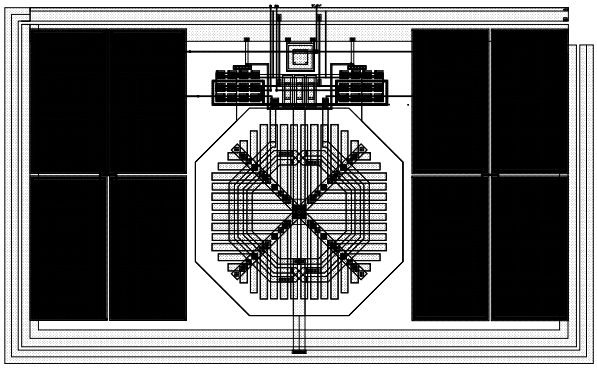

Fig. 6. Layout of the dual slope f2V converter.

If the expression for w_{in} is put in terms of center frequency of the f2V converter w_0 plus frequency change Δw and use the approximation $\frac{1}{1+x} \approx 1 - x$ for small values of x;

$$V(out) \approx \frac{w_{0_{f2}}^2 - w_{0_{f1}}^2}{w_0} \cdot L \cdot I_{LC} \cdot (1 - \frac{\Delta w}{w_0}) \quad (9)$$

If dual slope f2V converter gain is defined as,

$$K_{det} = \frac{w_{0_{f2}}^2 - w_{0_{f1}}^2}{w_0} \cdot L \cdot I_{LC} \quad (10)$$

then V(out) can be written as;

$$V(out) = K_{det} \cdot (1 - \frac{\Delta w}{w_0}) \quad (11)$$

It's seen from (11) that dual slope f2V converters give a linear transfer function proportional to input frequency change in the frequencies near the center frequency and they have a negative slope. The layout of the dual slope f2V converter is shown in Fig. 6. The output noise current floor of the designed detector is found as $0.27e^{-21}$ A^2/Hz for 184 mV/GHz detector gain.

B. Phase noise of the FLL

The noise contributions of each block will be added to find the noise contributions as seen in Fig. 7.

Forward gain of the loop is $K_{fwd} = K_{vco} \cdot H(s)/s$, where H(s) is the loop filter response. The loop gain is defined as $K_{loop} = K_{vco} \cdot K_{f2v} \cdot H(s)$. By using these definitions, noise transfer functions can be written as,

$$G_{vco} = \frac{1}{1 + K_{loop}} \quad (12)$$

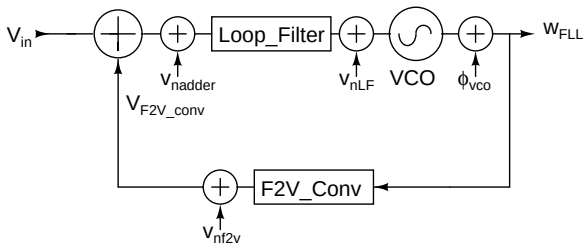

Fig. 7. Noise sources in a FLL

$$G_{f2V} = -\frac{K_{fwd}}{1 + K_{loop}} \quad (13)$$

$$G_{adder} = \frac{K_{fwd}}{1 + K_{loop}} \quad (14)$$

$$G_{LF} = \frac{K_{vco}}{1 + K_{loop}} \quad (15)$$

From noise transfer functions, it can be seen that in the bandwidth of the FLL, the noise from the VCO is suppressed substantially by the loop, but there are additional noise from the other elements of the loop, which are suppressed less. VCO and f2V converter are the most noisy components with most active elements and F2V converter noise is suppressed less than VCO phase noise.

In addition, it can be seen that the noise contribution from the adder is added to the frequency detector noise and have a strong effect on the loop noise, so as will be discussed in section IV, adder can be eliminated by current addition.

C. Simulations including f2V converter noise

After adding noise contribution of the dual slope f2V converter and adding the phase noise values of a moderate LC VCO, it can be seen from Fig. 8 that phase noise of the proposed VCO block is approximately 15 dBc/Hz less than the standalone VCO inside the FLL bandwidth.

During these simulations and investigations, it is observed that the phase noise of the overall VCO block depends heavily on the f2V converter noise performance and VCOs with much higher phase noise can be decreased to a similar phase noise value by using a low noise detector.

IV. Implementation of FLL inside a PLL

While implementing the FLL inside a PLL, main concern is the stability of the loops. Bandwidths of the loops should be well separated from each other, in order not to hurt the stability of the other. In this

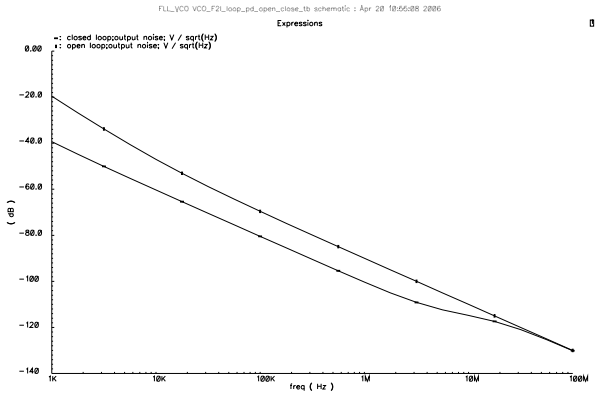

Fig. 8. Phase noise performance improvement using the dual slope f2V converter

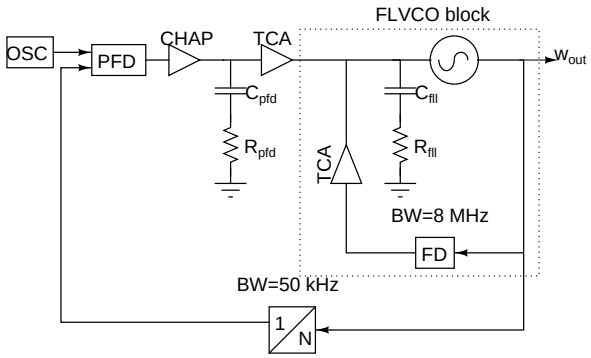

Fig. 9. Schematic of PLL including the FLL using TCAs

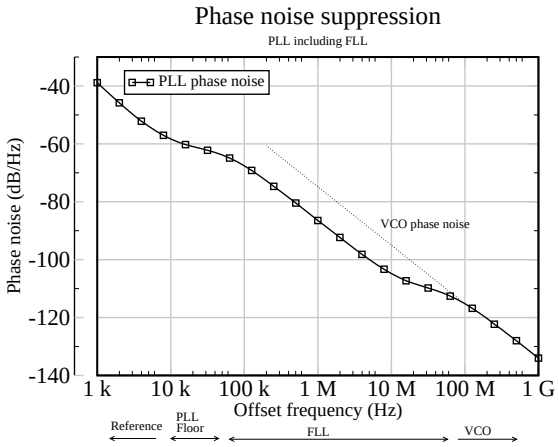

Fig. 10. Contribution of different blocks to PLL phase noise

implementation bandwidths are set 2 decades away from each other.

Two loops can be integrated either by a voltage adder that sums the output voltage of the phase frequency detector (PFD) filter and the f2V converter as demonstrated in the FLL schematics. Another way is using transconductance amplifier (TCA) to convert the output voltage of the PFD filter to a proportional current. By current addition in the connection point of the two loops, final current is sent to FLL filter. This can be implemented as seen in the Fig. 9. The choice between the configurations depends on the noise contribution values of voltage adder and TCA used after the PFD filter.

A. Loop transfer functions

F2V converter zero cancels the pole of the VCO inside the FLL, so the need for the zero realized by the loop resistor is not existent in the FLL. There is a filter after the PFD in the final implementation, so the FLL resistor in Fig. 9 can be omitted in calculations. By using the definition $K_{f2I} = K_{f2v} \cdot K_{TCA}$, FLL open loop transfer function is;

$$H_{FLL(OL)}(s) = \frac{K_{VCO} \cdot K_{f2I}}{C_{FLL} \cdot s} \tag{16}$$

As can be seen from (16), K_{f2I} and C_{FLL} can be used to set the bandwidth of the FLL, since K_{VCO} is same for both loops. Using (16), closed loop transfer function is;

$$H_{FLL(CL)}(s) = \frac{K_{VCO}}{s + \frac{K_{VCO} \cdot K_{f2I}}{C_{FLL}}} \tag{17}$$

The pole resulting from "VCO block" is not at zero, but at a frequency set by K_{VCO}, K_{f2I} and C_{FLL}. For the PLL, the only change is VCO transfer function, so the loop stability and bandwidth are not substantially affected by the proposed "VCO block". The loop is even more stable.

B. Simulation results

Fig. 10 shows the noise contribution of different dynamics in a PLL. As seen in the graph, the region, where the FLL is effective, is the frequencies higher than the PLL bandwidth up to offset frequencies inside the FLL bandwidth. Stand alone VCO phase noise is shown by dotted line in order to show the suppression by the FLL.

V. Conclusion

On-chip frequency locked loop (FLL) implementation over a VCO of a PLL is investigated, which is the first investigation published up to our knowledge. Advantages of linearity and phase noise suppression are demonstrated by both theoretical calculations and simulations using Verilog-A models including real noise values of the components. Final design is not implemented on chip yet, but it was proved by simulations that using this method, linearization can easily be achieved and phase noise suppression will be achieved depending on the noise of the VCO, especially on ring oscillators. Transistor level implementation of a special low noise f2V converter (frequency detector) without a reference frequency is also presented and a possible application of using FLL is also explained in introduction section to highlight the advantages.

Acknowledgment

Temporarily taken out for anonymous judging.

References

[1] J. Gustrau, F. Fiechtner, and M. Hoffmann, "VCO Linearisation by Frequency Feedback," in *IEEE Radio Frequency Integrated Circuits Symposium*, June 1998, pp. 135–138.

[2] R. B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee, and D. Leipold, "A Digitally Controlled Oscillator in a 90 nm Digital CMOS Process for Mobile Phones," in *Proc. IEEE International Solid-State Circuits Conference*, no. 11, Nov 2005, pp. 2203–2211.

[3] B. Giebel, J. Lutz, and P. L. OLeary, "Digitally Controlled 0scillator," in *Proc. IEEE International Solid-State Circuits Conference*, no. 6, Jun 1989, pp. 2203–2211.

[4] N. M. Pletcher and J. M. Rabaey, "A 100 μW 1.9GHz Oscillator with Fully Digital Frequency Tuning," in *Proceedings of ESSCIRC*, Sep 2005, pp. 387–390.